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SOSA and VITA: Working Together for Next-Gen Defense Systems

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IN THIS ISSUE

Introduction

The SOSA™ (Sensor Open Systems Architecture) Consortium is developing common open standards for designing, building, and deploying hardware, software, and firmware components of new military electronic systems. SOSA contributing members are U.S. government organizations including the U.S. DoD, Army, Navy, and Air Force, as well as key representatives from industry and universities.

SOSA™
Sensor Open Systems Architecture

SOSA adopts the most appropriate subsets of existing open standards to form a multi-purpose backbone of building blocks for current and future embedded systems for Radar, EO/IR, SIGINT, EW, and communications.

Objectives include vendor interoperability, lower procurement costs, easier new technology upgrades, quicker reaction to new requirements, and longer life cycles.

Because the emerging SOSA hardware standard draws primarily from OpenVPX and other related VITA standards, the new technologies, topologies, and environmental requirements critical to meeting SOSA objectives must be supported by extensions to these VITA standards.

VITA
Open Standards, Open Markets

This article is an overview of the SOSA and VITA organizations and how they interact, along with the challenges, successful strategies, and illustrative examples.

VITA Background & Mission

Introduced to the market in 1981, the VMEbus architecture began gaining market presence with specification development and products from Motorola and other early vendors, who formed the VMEbus Manufacturers Group (now VITA) in 1983.

In 1985, VITA (VMEbus International Trade Association) was founded to promote VMEbus in worldwide markets, and published its first directory of 174 vendor companies and over 2,700 product families. VMEbus soon won widespread acceptance and adoption by defense, government, research, and industrial customers.

The VITA Technical Committee, formed in 1987 to develop dozens of new extensions to VMEbus, evolved in 1994 into the present day VITA Standards Organization (VSO). A year earlier, VITA became an accredited standards development organization with the American National Standards Institute (ANSI).

To overcome performance limitations of the parallel bus backplane of VMEbus, in 2003 VITA introduced the VITA 46 VPX standard to take advantage of new gigabit serial interconnect technology for 3U and 6U boards. In 2010, after widespread use, refinements, and serious interest in VPX for long-term defense programs, VITA announced the VITA 65 OpenVPX system specification, quickly ratified by ANSI.

VITA continues its strong role in promoting and developing open architecture embedded system standards, actively supporting numerous working groups in the VSO, and working with vendors and other organizations to embrace new technology and meet new market requirements.

Open Systems Architecture Directive and Initiatives

In May 2013, the U.S. Under Secretary of Defense issued a milestone memo mandating that all acquisition activity must incorporate DoD Open Systems Architecture (OSA) principles and practices. These include using existing or evolving open standards for well-defined modular hardware and software components that can be sourced from multiple vendors. Once proven, hardware platforms should be reusable for quick-reaction mission needs, feature upgrades, and new technology insertion. Software architectures must be layered and extensible to permit operating system and security upgrades, and to accommodate new applications and user interfaces. These advantages reduce development risks and help ensure significantly longer operational life-cycles.

In response, each of the three primary U.S. service branches (Army, Navy, and Air Force), began developing standards that embraced OSA principles to meet future procurement needs of deployed systems for their respective services.

The Army's CCDC (Combat Capabilities Development Command) in Aberdeen, MD developed CMOSS (C4ISR/EW Modular Open Suite of Standards). These standards include OpenVPX for hardware, VICTORY to share vehicle services (like time and position) for C4ISR/EW interoperability, and MORA (Modular Open RF Architecture) to share antennas and amplifiers. It also uses REDHAWK and SCA software frameworks.

The Navy's NAVAIR (Naval Air Systems Command) in Patuxent River, MD created HOST (Hardware Open Systems Technology), which initially focused on embedded processing for airborne and ground vehicle missions. Its major goal of abstracting hardware and software components aligned well with OSA concepts. HOST hardware definitions include three tiers: Tier 1 defines the deployed platform (airframe, vehicle, UAV, etc.), Tier 2 defines the embedded system enclosure, and Tier 3 the boards, backplanes, modules, and faceplates. Tiers 2 and 3 are subsets of OpenVPX modules and profiles. A registry of Tier 3 products offers an approved catalog of components for sharing across programs.

The Air Force's OMS (Open Mission Systems) initiative incorporates SOA (Service Oriented Architecture) for commercially developed concepts and middleware, and UCI (Universal Command and Control Interface), which standardizes massages and middle-

ware for sharing command and control mission information between airborne system elements. OMS strongly embraces FACE (Future Airborne Capability Environment), a consortium of The Open Group that adopts open software standards for avionics systems, which gained full support of all three armed services.

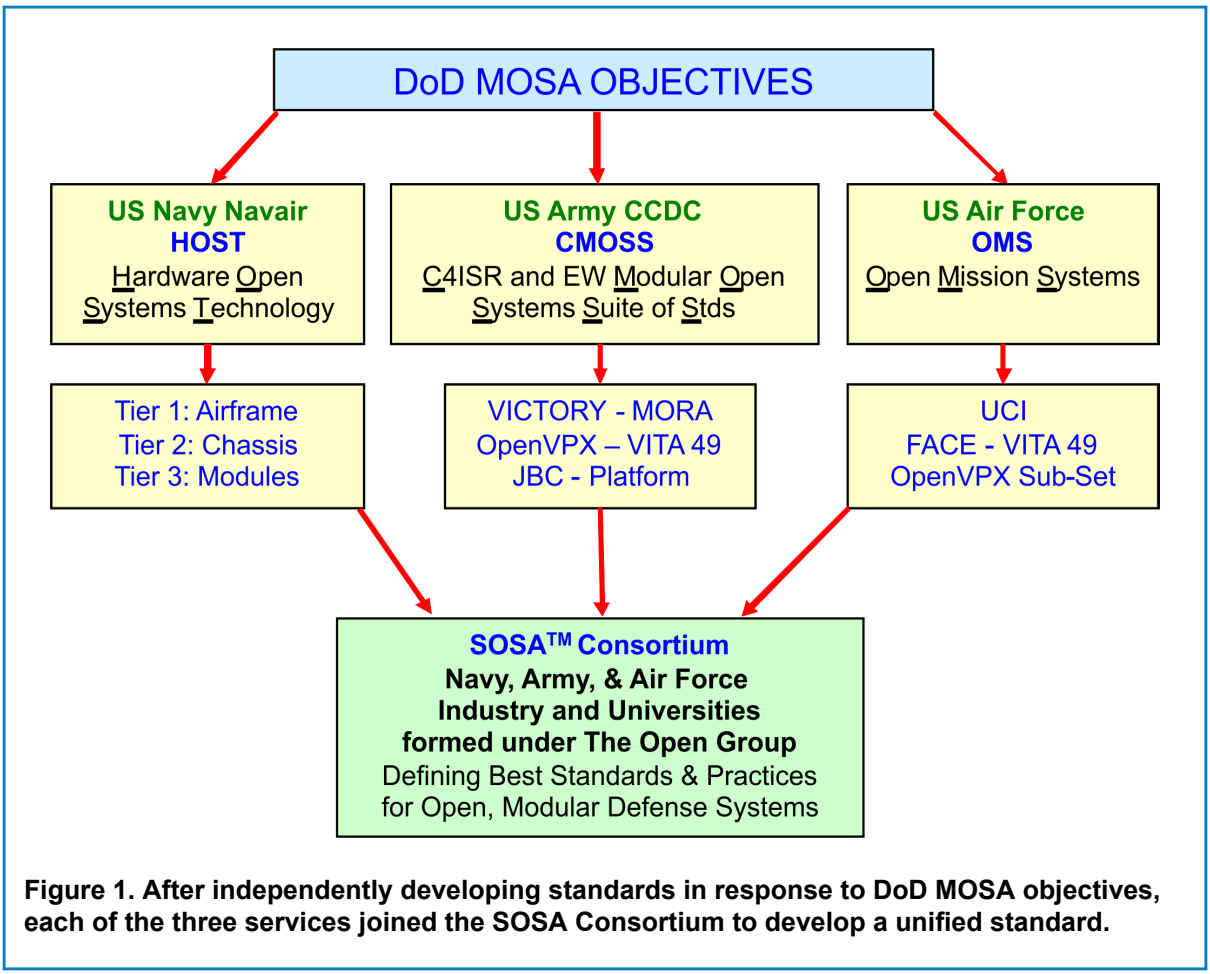


Figure 1. After independently developing standards in response to DoD MOSA objectives, each of the three services joined the SOSA Consortium to develop a unified standard.

SOSA Consortium

While each service made significant progress in advancing OSA principles, they did so through different initiatives that often shared common open standards, including OpenVPX and FACE. However, each initiative also included specific mandates tailored for service-specific platform requirements.

After recognizing these facts, administrators within DoD and each of the services perceived a strong need to promote a single, common initiative to define acquisition activities across all three services.

In early 2017, the DoD issued an SBIR solicitation for Sensor Open System Architecture (SOSA) Architectural Research outlining the numerous OSA initiatives and objectives for a unified solution. This resulted in the formation of the SOSA Consortium managed by The Open Group, a large organization with strict and well-defined practices, policies, and procedures for standards development efforts.

A primary mandate of the SOSA Consortium is broad participation, commitment, and contribution from DoD, Army, Navy, and Air Force, as well as industry, academia, and other government organizations. Major objectives include development and adoption of open systems architecture standards for C4ISR to provide a common, multi-purpose backbone for radar, EO/IR, SIGINT, EW and countermeasure systems. Additional objectives include platform affordability, rapid fielding, reconfigurability, new technology insertion, extended life-cycles, and re-purposing of hardware, firmware, and software.

Inside the SOSA Consortium

The SOSA Consortium Organization consists of two primary groups. The Business Working Group (BWG) defines business and acquisition practices, and creates guidance for acquisition programs. The Technical Working Group (TWG) is responsible for defining the SOSA Architecture, and producing the SOSA Technical Standard and SOSA Reference Design.

The SOSA Architecture presents a modular system structure, with tight integration within modules for encapsulating functionality and behaviors, and yet well-defined interfaces. These modules must be based on open, published standards, with consensus-based influence stakeholders directing the evolution, and a strict conformance validation process. The SOSA Architecture protects IP (intellectual property) within the modules to incentivize innovation and competition.

The SOSA Technical Standard documents the SOSA Architecture with detailed rules and requirements drawn and adapted from a collection of open standards. The primary standards

defining specifications for plug-in cards, backplanes, chassis, electrical components, and mechanical structures are VITA standards.

The SOSA Conformance Policy, now being defined by the SOSA Conformance Standing Committee, will define processes for qualifying products against the Technical Standard. They include multiple conformance verification processes, a single conformance certification process, and a single SOSA certified conformant product registration process. Until the award of certification, no product can claim to be SOSA conformant.

Membership in SOSA is restricted to US citizens and organizations so that DoD-sensitive or classified requirements can be presented by representatives from the armed services to promote solution strategies within the SOSA Technical Standard. For this reason, technical details of on-going discussions in the SOSA Technical Working Group may not be disclosed to the public. Once the standard is approved and released to the public, it will contain only specifications and rules, free from the underlying, sensitive use drivers.

VITA and SOSA

Because VITA is so central to the SOSA hardware definition, many of the same individuals in the SOSA TWG are also active participants in the VITA Standards Organization (VSO). Because restrictions on technical disclosures imposed on the TWG by SOSA do not apply to VSO, members of VSO must be mindful against referencing on-going SOSA technical topics in their VSO discussions and publications.

Nevertheless, the TWG does release period "snapshots" of the evolving SOSA Technical Standard that are publicly available for review, the latest being Snapshot 2 released in January 2020. While no conformance to these snapshots may be claimed, they illustrate the direction and underlying principles guiding the final standard.

In some cases, SOSA adopts only carefully selected subsets of existing VITA specifications. For example, the TWG adopted only a handful of the more than one hundred 3U and 6U OpenVPX slot and module profiles, based on an analysis that they could accommodate the majority of system requirements.

User-defined backplane pins defined in OpenVPX pose a nemesis for standardization efforts because they allow custom assignment of signals with interface standards, directions, and voltages. Profiles with user-defined pins are being deprecated in SOSA. Instead, work is underway to assign a minimum set of specific I/O standards to each group of legacy user-defined pins for each of the OpenVPX control, data, and expansion planes.

SOSA restricts the primary VPX power supplies to +12V only, prohibiting +5V, and +3.3V. This greatly simplifies the previous OpenVPX issue of balancing among three voltages to simplify chassis power supplies and standardize the plug-in cards.

Unlike most OpenVPX systems, SOSA requires hardware platform management leveraging the HOST 3.0 system management architecture, which itself is highly leveraged from VITA 46.11. A system manager module accesses all SOSA system elements for census taking, health monitoring, troubleshooting, new firmware/software upgrades, and reset/recovery operations.

Backplane I/O for RF signals and optical interfaces in OpenVPX have gained significant traction in CMOSS, MORA, and HOST systems over the last six years, all enabled by VITA 66 and VITA 67 specifications. Eliminating front panel cable harnesses wins high

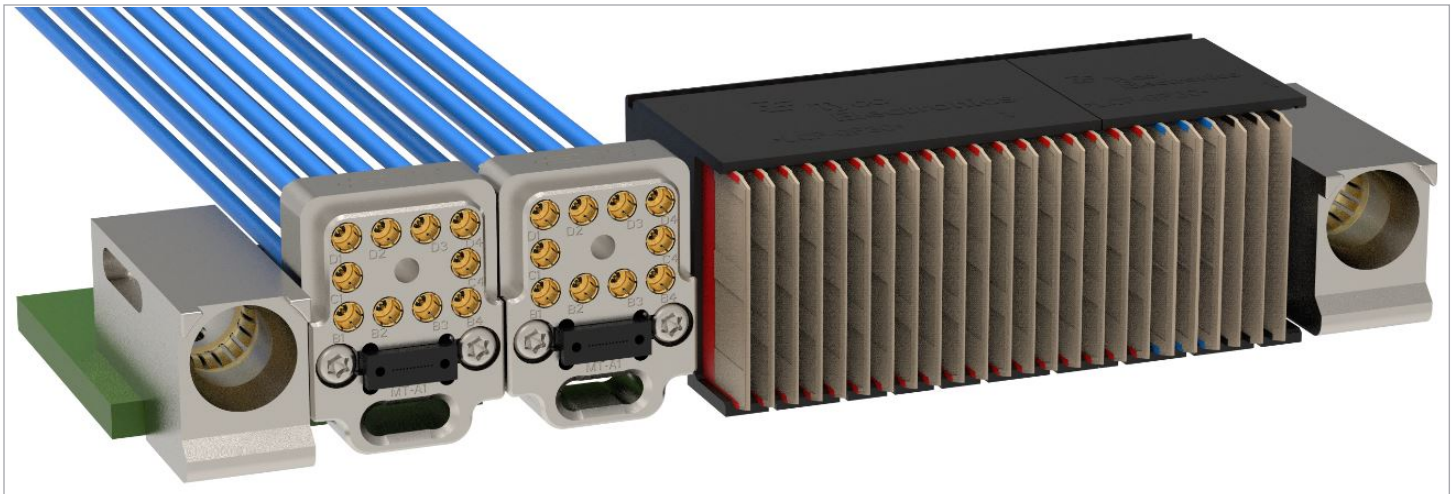


Figure 2. Rear view of 3U OpenVPX Module with two VITA 67.3D backplane connectors, each with 10 coaxial RF signals and 24 optical lanes. Courtesy TE Connectivity

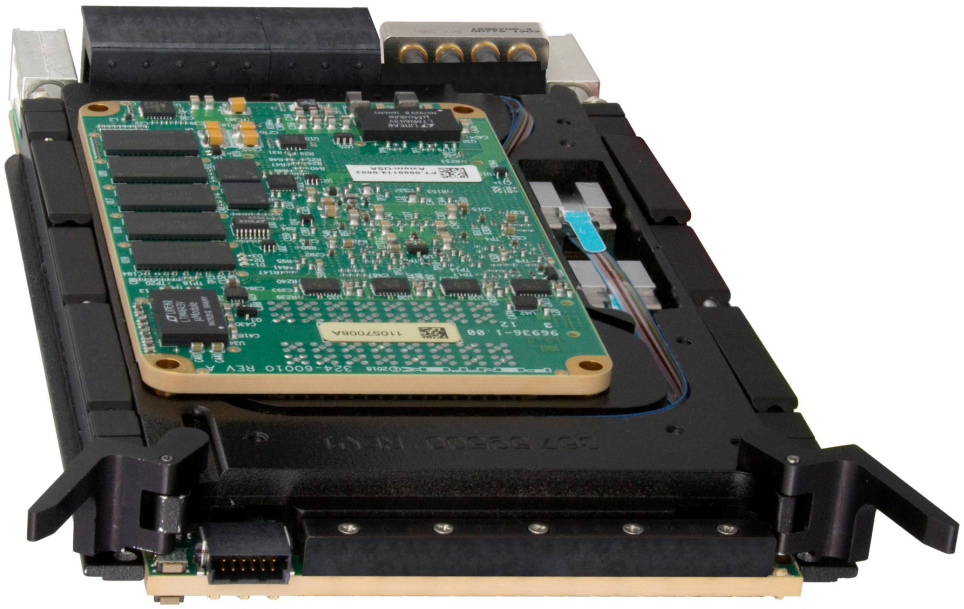


Figure 3. Pentek Quartz® Model 5550 3U VPX 8 Channel A/D and D/A RFSoC SOSA-Aligned Processor incorporates RF and optical backplane using VITA 66 or VITA 67 connectors. The top cover has been removed to show details.

scores for maintenance and reliability. Some of the latest modular backplane standards offer extremely high density and even mixed RF/optical interfaces as shown in Figure 2.

In summary, when critical needs arise from SOSA customers (DoD services), SOSA TWG members can promote innovation for new standards within the VSO to accommodate them, while still complying with SOSA restrictions.

Next Steps

The release of the Technical Standard Snapshot 3 is scheduled for early second quarter 2020, but the current public health crisis may delay this because of cancellations of face-to-face meetings. Nevertheless, web-based conferencing will augment the regular on-going conference calls to help maintain the momentum.

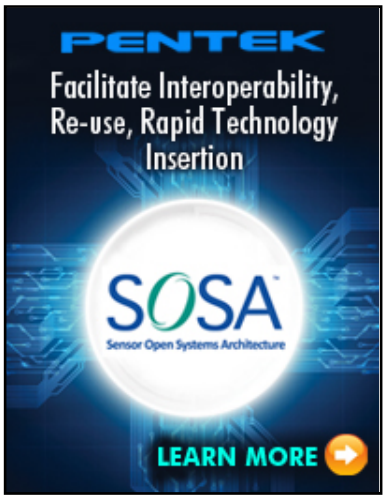
It is expected that the release of the SOSA Technical Standard 1.0 will be completed about nine months after Snapshot 3. At that point, product vendors may begin the processes leading to full certification.

Nevertheless, vendors are now offering products that were "developed in alignment with SOSA" like the one shown in Figure 3 (above). A key difference in the SOSA architecture from earlier open standards is the well-defined protection of IP, which encourages numerous examples of supplier innovation and investment.

The DoD is now issuing requests for proposals and information clearly favoring respondents that offer OSA-based solutions. The active participation in SOSA by the DoD, all three armed services, embedded industry vendors, universities, and research facilities gives evidence of their substantial commitments of resources and personnel. These clear signals ensure that SOSA is well on its way to revolutionize the future of embedded military electronics systems. □

Learn More About SOSA

For more information about SOSA, click the image below to go to Pentek's new SOSA web pages.



To listen to a McHale Report podcast about SOSA and more, click below.

Click the image below to download a new Pentek eBook that holds a compilation of articles about SOSA from *Electronic Design* magazine. □

Pentek Challenges SWaP Constraints with Rugged Small Form Factor Sentinel 26 GHz RF Recorder

- Ideal for SIGINT, COMINT, and ELINT applications
- Automatically tune, detect and record signals of interest from 1GHz to 26 GHz
- Capture instantaneous RF signal bandwidths up to 500 MHz
- ½ ATR chassis with front panel hot-swappable storage
- Removable SSD QuickPac® drive pack holds up to 61 TB of data

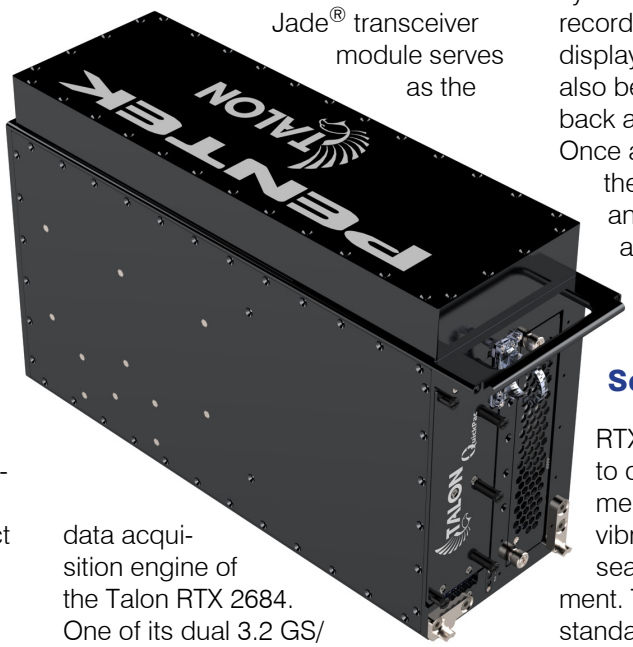
Pentek recently announced a major addition to its popular family of Talon® signal recording and playback systems: the RTX 2684 26 GHz RF Sentinel® Intelligent Signal Scanning small form factor recorder.

The RTX 2684 combines the power of a Pentek Talon Recording System with a 26-GHz RF tuner and Pentek's Sentinel intelligent signal scanning software, packaged in an extremely rugged, small form factor (SFF) 1/2 ATR chassis. Pentek's SFF recorders provide the performance of large rackmount recorders in the smallest footprint available in Pentek's Talon product line.

The Talon RTX 2684 SFF recorder weighs just 23 pounds and is designed for extreme operating environments. Optimized for SWaP (size, weight and power), the rugged sealed ½ ATR recorder is available with up to 61 TB of removable SSD storage. The ½ ATR chassis makes it highly suitable for military, security and government intelligence (SIGINT, COMINT, and ELINT) applications that are mobile or very space-limited.

SENTINEL

"The RTX 2684 Sentinel recorder is a complete antenna to disk solution with RF signals down-converted directly to the A/D converters," said Rodger Hosking, vice-president of Pentek. **"Its 5x reduction in packaging size over the rackmount equivalent, bandwidth performance, and storage capacity all offer huge improvements in addressing challenging SWaP constraints in mobile or space-limited platforms."**



A Pentek Model 78141 Jade® transceiver module serves as the data acquisition engine of the Talon RTX 2684. One of its dual 3.2 GS/sec 12-bit A/D converters operates at a sample rate of 2.8 GS/sec. The Model 78141 is coupled to the 500 MHz bandwidth analog IF output signal of a 26 GHz RF tuner front end, delivering excellent dynamic range across its entire spectrum. A digital downconverter (DDC) in the Model 78141 provides frequency zooming for recording signal bandwidths of 500, 250, or 125 MHz.

TALON RTX EXTREME RECORDER

Sentinel Intelligent Signal Scanning

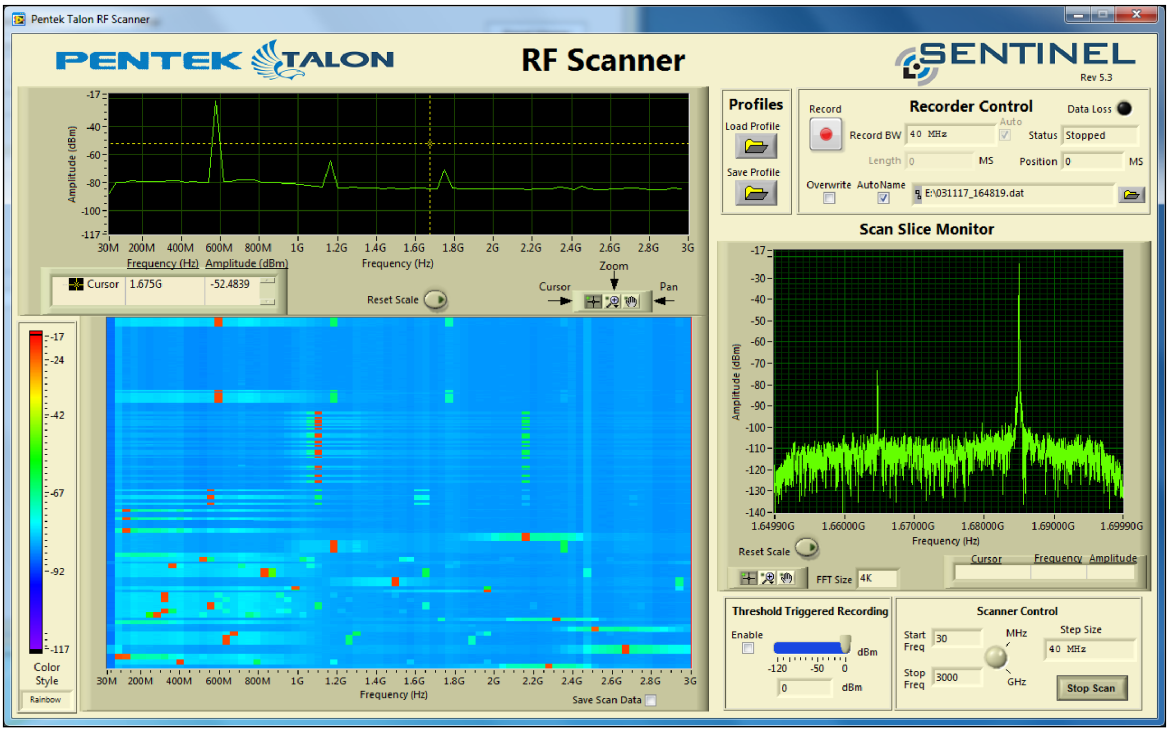
The RTX 2684 allows SIGINT engineers to scan the RF spectrum from 1 GHz to 26 GHz for signals of interest and monitor or record bandwidths up to 500 MHz wide. A spectral scan facility allows the user to scan the spectrum, while threshold detection allows the system to automatically lock onto and record signal bands. Scan results are displayed in a waterfall plot and can also be recorded so users can look back at some earlier spectral activity. Once a signal of interest is detected, the real-time recorder can capture and store terabytes of data to disk, allowing users to store data spanning many hours.

Extremely Rugged, Sealed Design

RTX SFF recorders are engineered to operate in the toughest environments with high levels of shock and vibration, plus all electronics are sealed from the external environment. The ½ ATR chassis uses military standard circular I/O connectors to control RF emissions while protecting the recorder's electronics from humidity, water, dust, sand and salt fog.

The Talon RTX SFF chassis seals the internal electronics from the outside environment by extracting heat through conduction to an air-cooled inner plenum. A thermostat-controlled, removable fan pulls air into the front of the chassis, through the plenum and then

out the back of the chassis. Only the fan is exposed to the outside environment, assuring all system electronics are protected in the sealed chassis. The inner plenum can be replaced to provide other cooling options, such as liquid or conduction cooling.



Designed to operate from -40°C to +50°C, these recorders can handle most thermal environments, making them ideal for UAV's, aircraft pods, tight equipment bays, military vehicles and most outdoor environments.

High-Speed Data Storage and Security

Pentek's QuickPac drive pack is easily removed from the recorder via a set of captive thumb screws on the front panel. Fully sealed with environmental gasketing, QuickPac drive packs can be quickly exchanged to support short down times and extended missions. A companion offload system for the QuickPacs is available so the recorder can be redeployed while the recorded data is transported and reviewed at a ground facility. The QuickPac drive pack holds up to 61 TB of SSD data storage and supports RAID levels 0, 5 or 6.

For secure applications, a separate operating system drive can be removed, allowing users to extract all non-volatile memory from the system in just a few seconds.

Mission Computer Capable

Talon RTX SFF recorders with the Intel Core i7 7700K, 7th Generation Quad Core 4.2 GHz processor and 8 GB DDR4 DRAM, are expandable to 16 or 32 GB with enough processing power to perform as the primary mission computer when needed, delivering state-of-the-art processing for mission applications and control, with minimal impact on the overall power budget of the system.

Ease of Operation

Sentinel recorders are built on a Windows workstation with an Intel Core i7 processor and provide both a GUI (graphical user interface) and API (Application Programmer's Interface) to control the system. Systems are fully supported by Pentek's SystemFlow® software for system.

control and turn-key operation. The SystemFlow software has been enhanced to include intelligent scanning and integrated control of the RF. The software provides a GUI with point-and-click configuration management and can store custom configurations for single-click setup. It also includes a virtual oscilloscope, spectrum analyzer and spectrogram to monitor signals before, during and after data collection.

Post processing and analysis software tools like Matlab can be installed on the Talon RTX 2684 platform. Data files are recorded to the Windows native NTFS file system, which allows operators immediate access to recordings without the need for any file format conversion.

Available Options

The Talon SFF recorders offer an optional GPS receiver for precise time and position stamping. Additional QuickPac drive packs with 3.8 to 61 TB are available. Computer I/O on all models includes Gigabit Ethernet, USB 3.0 and HDMI.

For more information about Pentek's Talon recording systems, click here.

You also can email us at sales@pentek.com, contact your local representative, or contact Pentek directly [+1 (201) 818-5900]. □

Pentek Launches Revolutionary ArchiTek FPGA Development Suite for Talon Recorders

- Complete development environment to add custom FPGA IP to Talon RF/IF signal
- Ideal for SIGINT, COMINT, and ELINT applications
- Fully integrated with Pentek's Navigator® Design Suite
- Fully compatible with Xilinx's Vivado® Design Suite

Custom FPGA IP designs ...

- Allow recording of only critical data
- Reduce or eliminate post-processing requirements
- Reduce storage capacity requirements
- Reduce data offload time
- Provide additional record/play channels

Pentek recently announced its ArchiTek™ FPGA Development Suite, a revolutionary product for adding custom IP to select Pentek Talon® recording systems. ArchiTek is a comprehensive development environment that enables engineers to add FPGA IP to recording systems, such as threshold detection, spectral filtering, digital down-conversion, signal classification, demodulation and many other digital signal processing techniques.

Developing custom IP for an FPGA requires an architecture that protects the user from custom IP development pitfalls such as breaking the existing IP and corresponding recording software. ArchiTek harnesses Pentek's Navigator FPGA Development Kit (FDK) and Board Support Package (BSP) to provide a development environment that steps engineers through the process of integrating custom IP into the recorder.

Along with the Navigator FDK, ArchiTek provides the foundation and example projects for adding IP to user blocks and creating additional data-path branches from existing data streams. The structured design protects the recorder's standard functionality, reducing development time and risk.

"Pentek has structured FPGA designs in a way that allows engineers to easily add digital signal processing IP to our signal acquisition boards," said Chris Tojeira, Pentek's recording systems director. **"ArchiTek extends this capability to our Talon recorder product line, resulting in a customizable instrument that better targets the user's application."**

Customers can now add FPGA IP to a recorder for real-time, on-the-fly digital signal processing during the data acquisition process, greatly reducing the time associated with post-processing recorded data. Recording of only critical data also greatly reduces transfer rates, recording capacity requirements, and data offload time.

Using ArchiTek, FPGA developers can add additional recording channels to the system, so users can record both processed and unprocessed data simultaneously. ArchiTek provides extensive documentation and tutorials to assist developers through the customization process, reducing both risk and development time.

ArchiTek Use-Case Examples

Many digital communication protocols use spread-spectrum techniques, in which many signal channels are spread across the same frequency span using pseudo-random sequence encoding. Instead of recording the entire frequency span, ArchiTek allows one signal of interest to be extracted using a custom FPGA block so that only that signal is delivered for recording. This can reduce the recording rate and storage capacity by orders of magnitude.

Another SIGINT monitoring application might require signal classification and time stamping of each received transmission. By suitably configuring the classification algorithm within the FPGA using ArchiTek, only the key parameters of each signal need to be recorded instead of the signals themselves, thus dramatically extending the useful mission time. This strategy of real-time processing at the front end also reduces or eliminates post-processing tasks.

For more information ...

For more information about ArchiTek, click here.

For more information about Pentek's Talon recording systems, click here.

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Pentek's Four-channel, 1.25 GHz D/A Jade Architecture XMC Ideal for Waveform Generation

- Jade® architecture with Xilinx® Kintex® UltraScale™ FPGA offers price, power, and processing performance advantages
- Four D/A waveform generator IP modules for simplifying data playback
- Navigator Design Suite speeds development and custom IP integration

The Jade Model 71871 combines two Texas Instruments DAC 3484s to deliver four independent analog outputs, each through its own digital upconverter and 16-bit D/A with sampling rates to 1.25 GHz. A Xilinx Kintex Ultrascale FPGA contains factory-installed functions that include a sophisticated D/A Waveform Generation IP module. It allows users to easily deliver waveforms stored in either on-board memory or off-board host memory to the four D/As. Complex output waveforms, each with bandwidths up to 250 MHz, can be independently translated to programmable IF frequencies.

"The Jade Model 71871 builds on the capabilities of the popular Jade line of XMCs," said Robert Sgandurra, director of Product Management. **"Pentek's Navigator® Design Suite adds more IP with each product release, all of which is fully available to our customers for even more effective product development."**

The Model 71871 can be configured with a range of Kintex UltraScale FPGAs to match specific requirements of the processing task, spanning the entry-level KU035 (with 1,700 DSP slices) to the high-performance KU115 (with 5,520 DSP slices). The KU115 is ideal for demanding beam-forming, modulation, encoding, and encryption of the signals prior to transmission. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

A pair of front-panel ¼ Sync connectors allows multiple modules to be synchronized. The Model 71871 can be optionally configured with a P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O to the carrier board. An optional P16 XMC connector adds an 8X gigabit link to the FPGA to support serial protocols.

The Jade Architecture

The Pentek Jade architecture is based on the Xilinx Kintex UltraScale FPGA, which raises digital signal processing (DSP) performance by over 50% over the previous family, with equally impressive reductions in cost, power dissipation and weight. As the central feature of the Jade Architecture, the FPGA has access to all data and control paths, ➤

enabling factory-installed functions including data multiplexing, channel selection, data unpacking, gating, triggering and memory control. A 5 GB bank of 2400 MHz DDR4 SDRAM provides on-board storage of waveforms for output through the D/As.

Navigator Design Suite

Pentek's Navigator Design Suite was designed from the ground up to work with Pentek's Jade architecture and Xilinx's Vivado Design Suite, providing an unparalleled plug-and-play solution to the complex task of IP and control software creation and compatibility. Graphical design entry for Xilinx and Pentek AXI4-compliant IP modules using the Xilinx IP Integrator greatly speeds development tasks.

The Navigator Design Suite consists of two components: Navigator FDK (FPGA Design Kit) for integrating custom IP into Pentek sourced designs and Navigator BSP (Board Support Package) for creating host applications. Users can work efficiently at the API level for software development and with an intuitive graphical interface for IP design. The Navigator BSP is available for Windows and Linux operating systems.

For more information about Jade Model 71871, click here.

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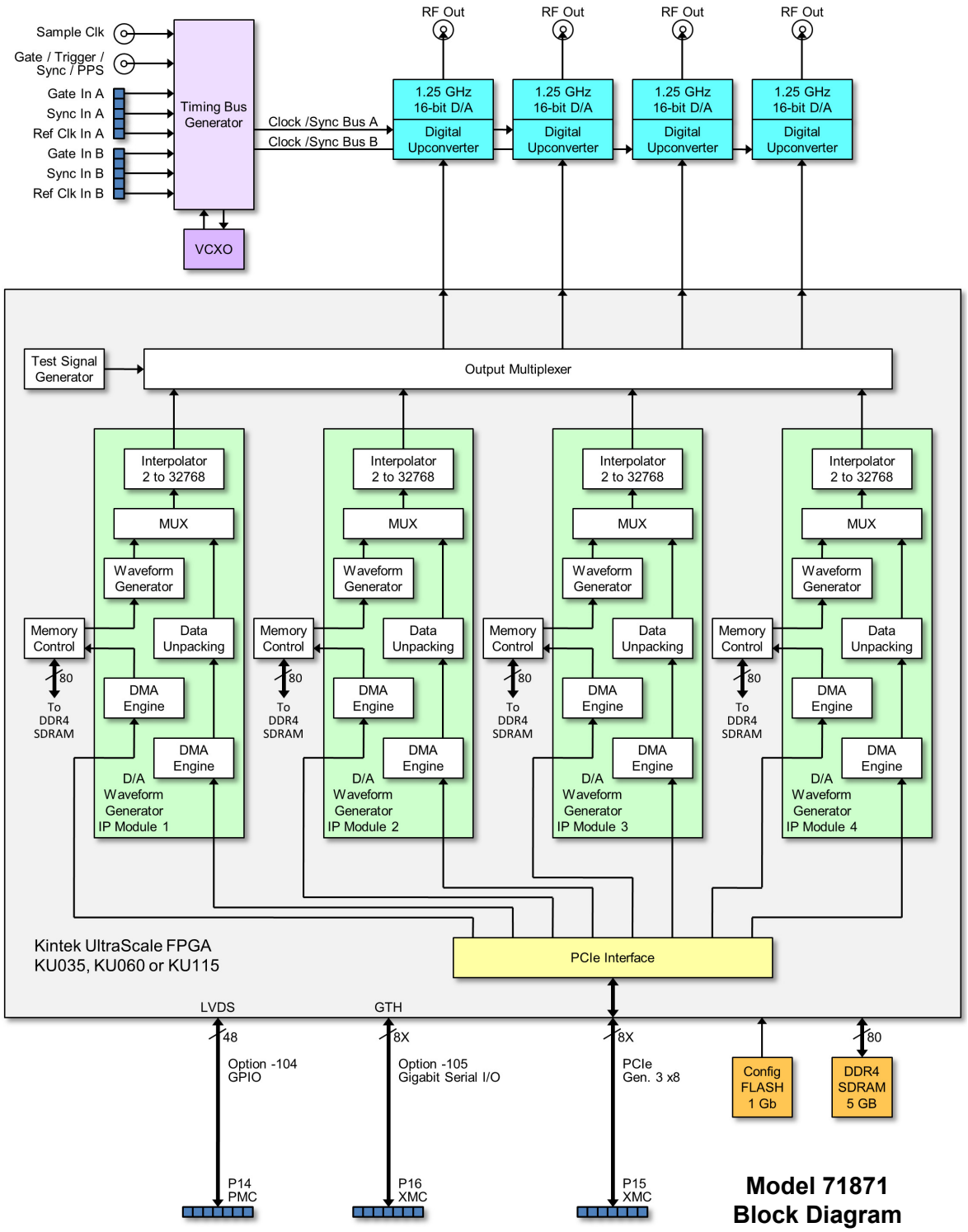

Model 71871 Block Diagram