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In This Issue

"RFSoC brings new possibilities for addressing some of the most challenging requirements of high-bandwidth, high-channel-count systems. Understanding how this new technology can specifically address SWaP-C and low latency applications is key to matching it to many applications that can benefit from it the most."

Bob Sgandurra, Director, Product Management, Pentek

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Strategies for Deploying Xilinx's Zync UltraScale+ RFSoC

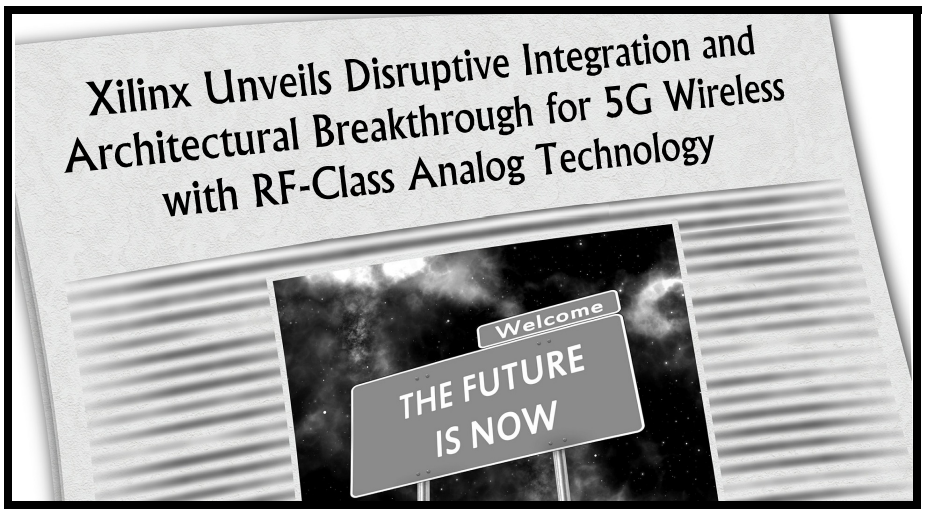
by Bob Sgandurra

On February 21st, 2017, Xilinx® announced the introduction of a new technology called RFSoC with the rather dramatic headline "***Xilinx Unveils Disruptive Integration and Architectural Breakthrough for 5G Wireless with RF-Class Analog Technology.***" The proposition was simple: add RF-class analog to digital and digital to analog data converters to Xilinx's already powerful MPSoC, ARM processor enhanced family of high performance FPGAs. And while the concept was simple, the implications were profound, changing the way engineers could design and package small, high channel count systems. And this technology not only offers new possibilities for 5G applications, but has significant impact in military and scientific systems, justifying the claim in Xilinx's announcement. To get better appreciation of the capabilities of RFSoC and understand how to best use the advantages of this technology, it's worth taking a quick look at current trends in data converters and signal processing.

What is RFSoC?

RFSoC, or more properly, Zynq® UltraScale+™ RFSoC, is based on Xilinx's prior family, the Zynq UltraScale+ MPSoC. The MPSoC is a system-on-chip architecture that includes up to four ARM Cortex-A53 application processors and two ARM Cortex-R5 real-time processors integrated into the UltraScale+ programmable logic. This solution offers the software programmability and flexibility of a processor with the hardware programmability and performance of an FPGA in a single IC.

RFSoC builds on the MPSoC foundation and adds eight 4 GSPS 12-bit A/Ds, each equipped with programmable Digital Downconverters (DDCs) and eight 6.4 GSPS 14-bit D/As, each equipped with Digital Upconverters (DUCs). While other A/D and D/A configurations are available, we'll consider the eight A/D and eight D/A configuration for the rest of this article. **Figure 1** shows the similarity between the MPSoC and RFSoC. ➢



Improvements in SWaP and Cost

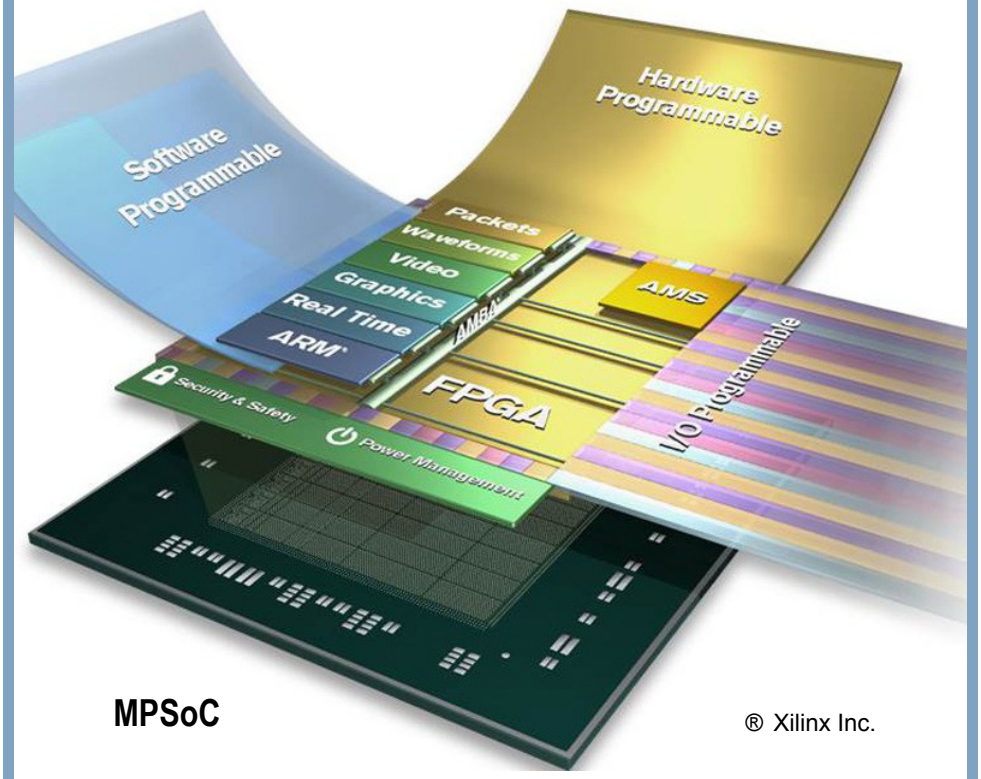
A common term in military applications is SWaP, which stands for Size, Weight and Power and refers to the ongoing requirement to reduce these attributes for communications, reconnaissance, radar and various types of signal acquisition and processing systems. The need for smaller, lighter, and use of less power becomes obvious when you think about where these systems are often deployed. Unmanned vehicles like unmanned aerial vehicles (UAV) and unmanned underwater vehicles (UUV) frequently require stealth to achieve their mission. Smaller, lighter and use of less power usually equates to stealthier, enabling these systems to be more effective.

Manpack (or womanpack) systems where the communications or direction-finding equipment and its associated power supply are worn by personnel are another target for SWaP reduction. Here again, smaller, lighter and use of less power is needed for making a practical, human-carried system.

RFSoC's high level of integration provides a significant amount of SWaP reduction when compared to designing the same functionality with discrete components. **Figure 2** shows the reduction in size by representing component footprints graphically. In the comparison, each component is roughly to scale, and space has been left between the discrete components to model a typical PCB layout, where ICs need space between them for assembly and placement of passive components. The RFSoC implementation can save 50% or more in overall size compared to the discrete approach.

While RFSoC can reduce weight at the component level, that savings is minimal when you consider the total weight of nine ICs compared to a single RFSoC. Where weight savings can be appreciated is when you look at power. With each watt of power in a system comes the weight of a cooling solution, either in metal or composite heatsinks, or in some systems, ➢

Figure 1. Xilinx's Zynq UltraScale MPSoC versus RFSoC



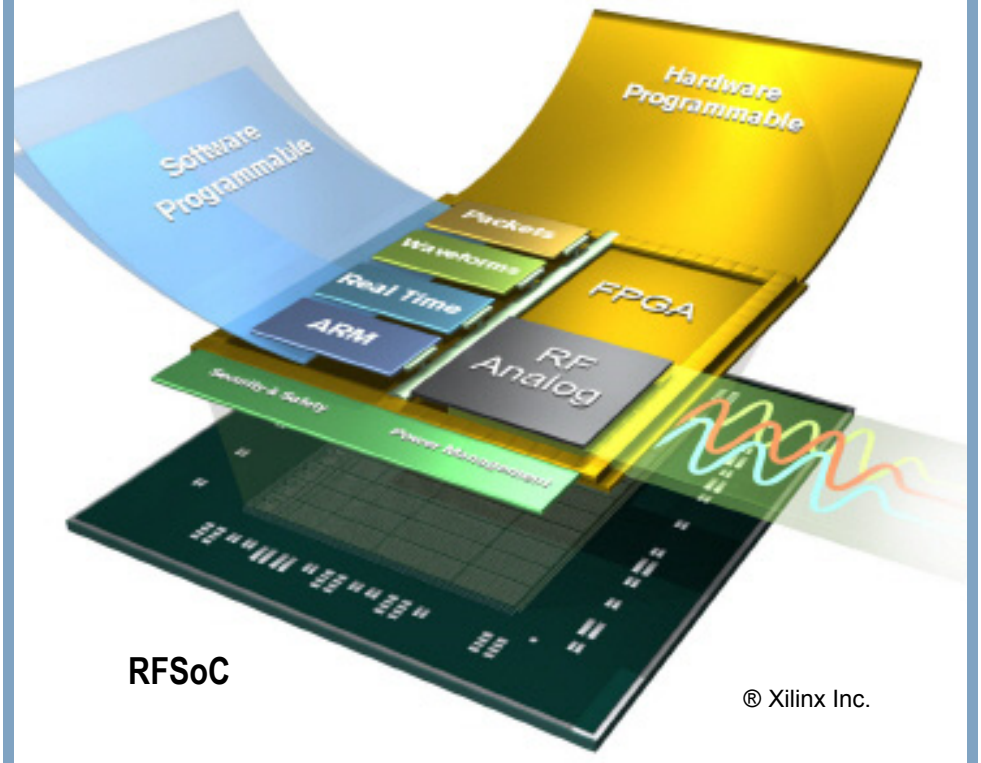
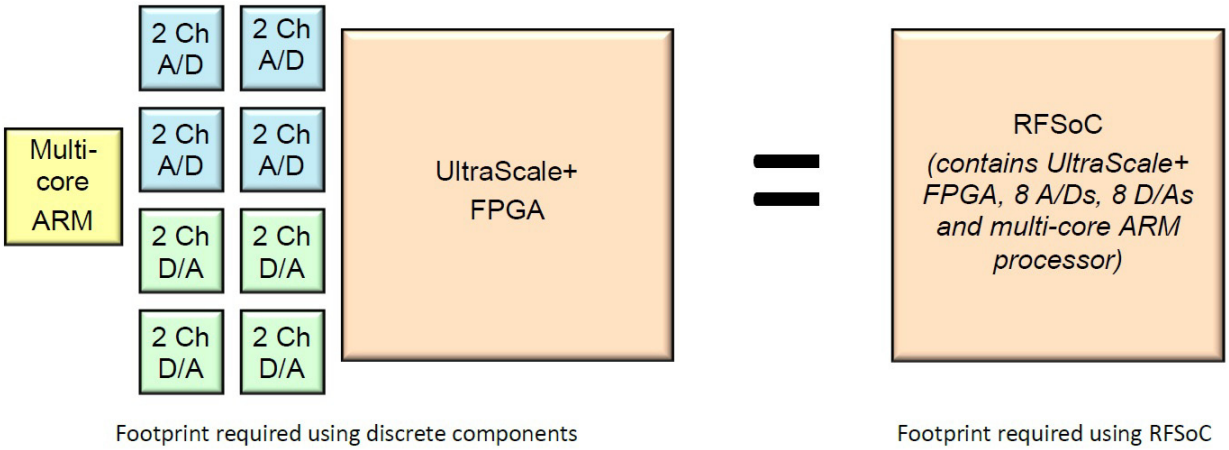


Figure 2. Discrete component versus RFSoC solution size comparison



more exotic solutions like liquid and vapor cooling. RFSoC can easily bring power savings of 30% to 40% or more compared to typical discrete solutions, thereby reducing the cooling solution's complexity and weight. And in portable systems, every watt that can be eliminated results in smaller, lighter batteries and longer operation time.

A key reason for the reduced power of RFSoC is the elimination of the interfaces needed to connect the various ICs in a discrete solution. Most data converters sampling at 1 or 2 GHz or higher depend on serial interfaces to move digital data between the converter and the FPGA. These interfaces expend power at both the data converter side and the FPGA side in serializing and deserializing (SerDes) circuitry. The most common serial interface protocol used for converters is JESD204.

By integrating the converters directly into the FPGA, the serial interfaces are eliminated as well as data transfer latency which the SerDes process and protocol introduce. (More on serial vs. parallel converter interfaces and latency later in this article.)

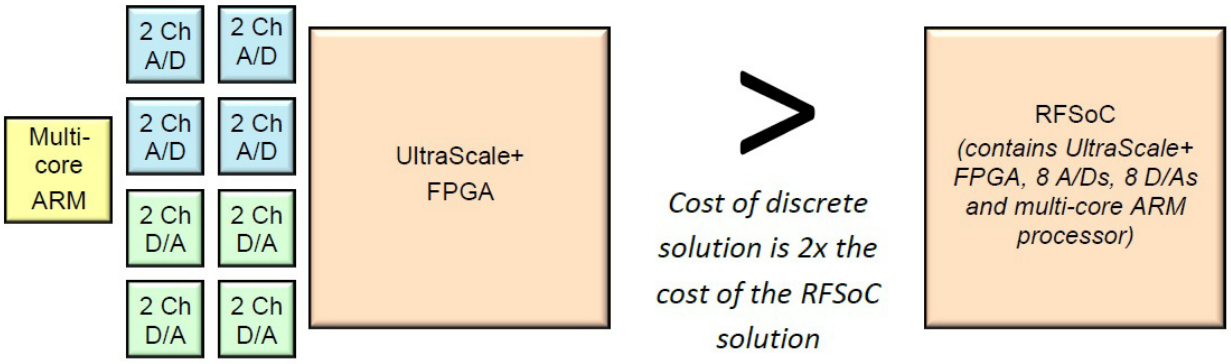
Another parameter often tacked onto SWaP is cost, sometimes referred to as SWaP-C. Here again RFSoC address the requirement. The same comparison used earlier of implementing the functions of the RFSoC as discrete components yields the following results (see **Figure 3**):

The cost of a typical multi-core ARM processor + (4 x Dual 4 GSPS A/Ds) + (4 x Dual 6.4 GSPS D/As) + Kintex UltraScale+ FPGA (with equivalent programmable logic and DSP density of the RFSoC) = approximately 2x the cost of the same functionality delivered in a single RFSoC.

While savings at any level is always welcome, the real benefit of the reduced cost can be seen in systems where many channels of A/Ds and D/As are required. Massive multiple-input multiple-output (MIMO) antennas are being targeted for applications from Wi-Fi to LTE to 5G. Massive MIMO antennas typically start at 8x8 configurations (8 receive channels and 8 transmit channels) and can be multiples of that configuration. This is a perfect match for the converters in the RFSoC.

Another high-channel-count application is phased array radar. The Multi-function Phased Array Radar (MPAR) initiative combines the functions of several national radar networks into a single system for aircraft and weather surveillance. It is not uncommon for these antenna arrays to be specified with 64 or more elements, with each element requiring an ➢

Figure 3. Discrete component versus RFSoC solution cost comparison

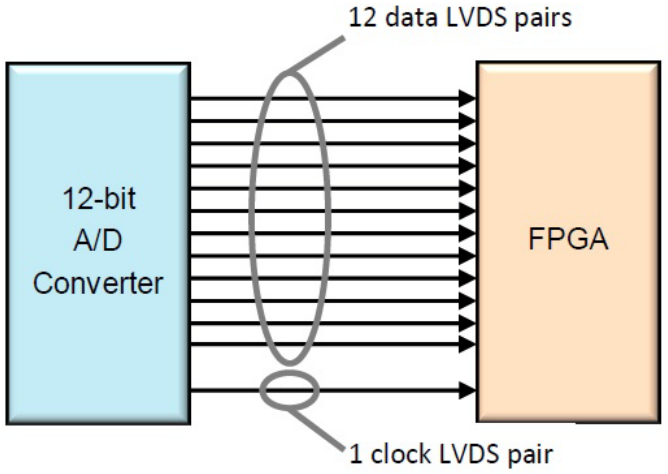


A/D and D/A pair combined with signal generation and receive and control processing. With these systems as well as military surveillance and targeting systems where hundreds of elements can be required, the savings found in RFSoC's integrated solution can add up quickly.

Data Converter Interfaces

Up to this point, the advantages of RFSoC have been primarily in improving on already available solutions: saving on size, weight, power, and cost compared to discrete component solutions. But by integrating the data converters into the FPGA, RFSoC offers a solution that is currently unavailable using existing technology. To understand this you must first look at how data converters connect to FPGAs. Using A/Ds as an example (but this is the same for D/As), connecting a 12-bit A/D to an FPGA using a parallel interface might look like Figure 4, where each bit is represented by an LVDS pair and an additional pair is used for data ready or clock.

Figure 4. A/D converter to FPGA interface using parallel LVDS pairs



In some cases, the interface can make use of double data rate (DDR) technology where data is transferred on the rising and falling edge of the clock, effectively doubling the amount of data transferred in a single clock cycle. But even with DDR, parallel converter interfaces become problematic for data converters with sample rates above about 1.5 GHz due to the speed limitations of the LVDS interfaces on FPGAs. To overcome this, one solution is to use a 1:2 demultiplexed interface (DeMux) where data is sent over two parallel interfaces, each running at half of the sample rate. In the 12-bit A/D converter example, if the converter is sampling at 2 GHz, each of the 12-bit paths following the DeMux are running at 1 GHz. This keeps each 12-bit interface below the maximum clock rate allowed by the FPGA LVDS interface but still delivers the data needed to support the 2 GHz sample rate (see Figure 5).

But this solution also becomes problematic at higher speeds. Using this same technique, a 4 GHz A/D would require a 1:4 DeMux. This quickly starts to become a PCB design challenge when you consider the number of pairs needed and that these signals need to be critically routed to maintain tight length matching between pairs so data arrives at the FPGA across all 12 bits at the same time. In addition to the routing challenge, a 12-bit A/D converter now requires 4 sets of 12 pairs (or 96 individual I/O pins, not including clock pins) to interface to the FPGA. In a typical FPGA device where 400 to 600 I/O pins might be available for interfacing all parallel devices like A/D and D/A converters and memory, half the pins could easily be used to connect just two 4 GHz A/D converters. ➢

Figure 5. A/D converter to FPGA interface using a 1:2 DeMux

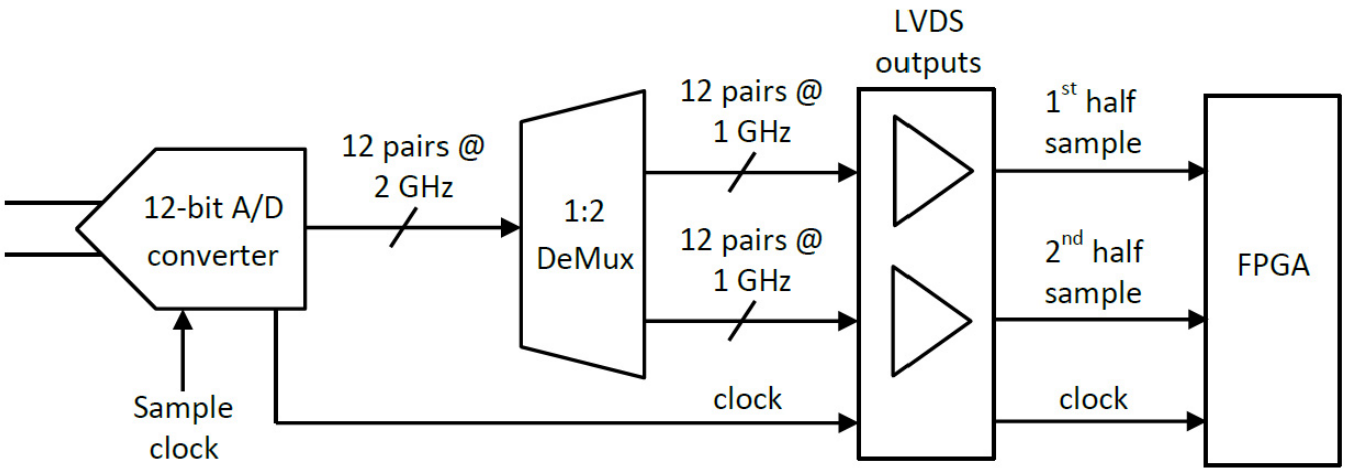
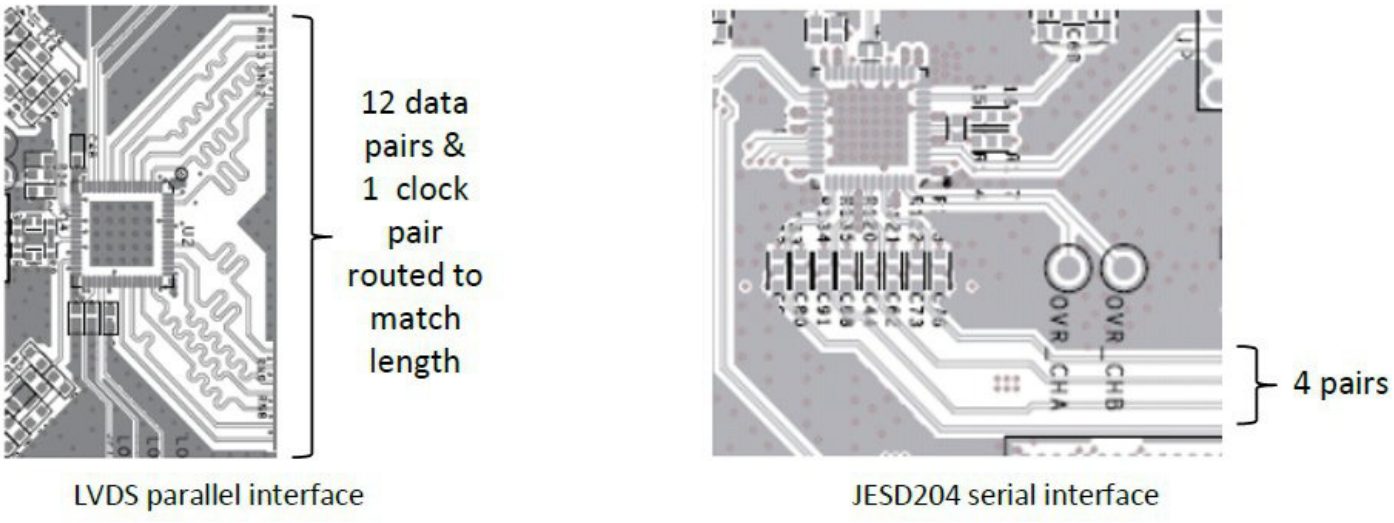


Figure 6. Parallel versus serial PCB routing



An alternate solution to the high-pin-count interface is to use a serial interface to connect data converters. JESD204 was created for this exact purpose. JESD204 makes use of the FPGA gigabit serial interfaces instead of LVDS. **Figure 6** shows a PCB routed for a 1 GHz 12-bit A/D connected via parallel LVDS and a PCB routed for a similar 1 GHz 12-bit A/D connected via four high-speed serial interfaces (or lanes) using JEDS204. The four lanes pose less of a PCB design challenge because of the reduced number of signals as well as the fact that the interface standard includes clock and data recovery features which eliminate the need to critically match the length of all lanes.

So while JESD204 can be a good solution for many high-speed data converter applications, it's not a perfect solution. The JESD204 IP and gigabit serial interface add about 1W to the power budget for every four lanes used. JESD204 is a proprietary IP core and typically requires a paid license to use it. In addition, using JESD204 can add complexity to the FPGA IP design. In applications where multiple converters across multiple ICs need to be synchronized, JESD204 requires a more elaborate clocking solution than parallel interfaces adding some additional circuitry and complexity. But while each of these obstacles can add power, cost, complexity and increased size, none is typically a showstopper.

Where JESD204 becomes a true impediment for some applications is in link latency. Where a parallel converter interface can delay the data by, at most, a few sample clock cycles for local buffering, the JESD204 protocol and the SerDes required to support it can add 80 sample clock cycles or more of latency from when the data is converted to when it is available in the FPGA for an A/D converter and in the reverse direction for a D/A converter. In some applications where data is streamed and processing results are not required in real-time, this poses no problem. As long as the data arrives at the FPGA without losing any samples, how long it takes to get there is not critical. But in many applications, including high-speed, tight control loop systems, some radar systems, and electronic warfare like countermeasures, where there is a very short time allowed for acquiring the data, processing it and turning it around, this latency eliminates JESD204-based solutions.

So, what does all this have to do with RFSoC? With the data converters integrated directly into the FPGA using parallel interfaces, they don't require the prohibitively high-pin-count external connections needed for discrete parallel interface converters, allowing more converter channels to be supported by a single FPGA. In addition, it does not have the latency associated with a JESD204 serial interface. This makes RFSoC an attractive solution for high-channel-count and low-latency applications.

Hardware Design with RFSoC

The circuit density and small size of the RFSoC create some unique challenges for circuit and PCB designers when engineering systems using the FPGA. Designing and laying out the PCB for the analog interface containing 16 channels (8 A/D and 8 D/A) requires attention to even the smallest details, to maintain signal quality and reduce crosstalk in such a dense configuration. Similarly, the RFSoC's GTYs (gigabit serial interfaces) are capable of running at higher than 32 Gb/sec. This poses another layout and routing challenge to the PCB design to maintain these speeds with signal integrity. For some operating modes, the RFSoC requires up to nine different supply voltages. Add to that another four or five supplies for peripheral circuitry and the power generation and management design can become complex very quickly. While each of these challenges can be demanding on its own, consider that many of the applications where RFSoC can bring the greatest ➢

benefit are in space-restricted and harsh environments, exacerbating the design challenge.

At Pentek, we have taken a unique approach to delivering RFSoC functionality to our customers. Our Model 6001 QuartzXM™ RFSoC eXpress Module is a small 2.5" x 4" board containing the Zynq UltraScale+ RFSoC FPGA and all peripheral and power circuitry needed for support and operation (see **Figure 7**). The concept behind the QuartzXM is simple: to provide the RFSoC functionality in a small, fully designed package that can be used on different carriers as needed to match the specific interface requirements of different applications. By offering the RFSoC on the QuartzXM, Pentek is delivering not only the RFSoC functionality, but is delivering a solution where many of the most demanding circuitry and packaging challenges have been solved.

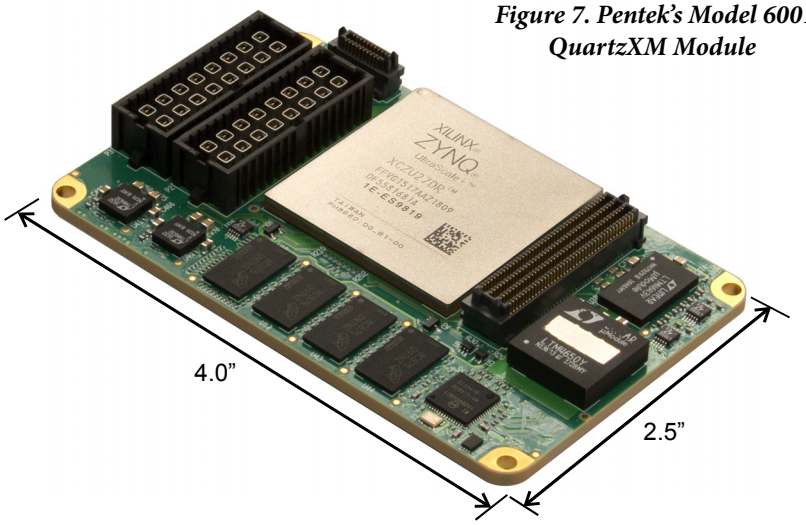


Figure 7. Pentek's Model 6001 QuartzXM Module

Figure 8. Pentek's Model 5950 Quartz 3U VPX Board, conduction-cooled version, with top cover removed to show the Model 6001 QuartzXM Module

Our Quartz™ line includes board products in standard from factors like 3U VPX (see **Figure 8**) and PCIe, delivering the QuartzXM in turn-key solutions ready for immediate deployment. The products are available in commercial and rugged, conduction-cooled versions, and in many situations this will be the final deployed solution. But with the modular design of QuartzXM, the standard form factor board can be the platform where the application is developed and proven, and then the QuartzXM module can be migrated to a custom carrier platform for deployment. More information about Pentek's Quartz products can be found here: **https://www.pentek.com/go/pipeRFSoC**

Software and IP Design

With each new family of FPGA, there has been a constant progression towards more powerful processing solutions. Each new family adds more logic density, faster logic fabric, more DSP resources, more on-chip memory, faster interfaces, and now with RFSoC, high-sample-rate A/D and D/A converters. While these new capabilities are certainly welcome, and they do enable more and more complex applications to be targeted at FPGAs, they also raise the bar for better and more capable design tools to handle the increasing complexity and size of the new IP that can be created.

Xilinx has addressed the design tool challenge with their Vivado® Design Suite. It includes tools for every aspect of the design cycle. The latest version has improvements in performance, with faster routing and more efficient FPGA resource usage, allowing denser designs. Vivado also addresses the increasing design complexity challenges with tools for creating processing IP with C-language specification, an integrated software development kit that targets the ARM processors, and plug-and-play block-diagram-based IP integration with IP Integrator. While all ➢

these tool improvements go a long way in enabling both software and IP engineers, the job of creating a complete system solution can be greatly accelerated when manufacturers of FPGA based hardware products provide IP and software libraries to support the specific features of the hardware. The better the foundation of software and IP that the manufacturer provides for the engineer to build an application on, the faster the engineer can complete the job of producing a final, robust system.

All Pentek hardware products include a full suite of FPGA-based functions, allowing the product to be used immediately in a range of applications without the need to create any FPGA IP. For all of our A/D or D/A-based products, the functions can include data acquisition and waveform generator engines, data tagging and metadata creation, VITA-49 packet creation, digital downconverters, multi-channel and multi-board synchronization, and optimized DMA for moving data on and off board through PCIe or 10GigE, in addition to IP targeted at specific applications.

RFSoC again brings new challenges and solutions with the sheer amount of data the A/D and D/A converters can introduce and the minimum latency interfaces between data converters and programmable logic in time-critical applications. Pentek's Quartz products address some of the most common requirements of RFSoC-targeted applications with new built-in IP ready to use with no additional IP design needed. These include an enhanced acquisition engine that supports the full bandwidth 4 GHz sample rate with options to snapshot data to on-board memory or to stream over dual 100 GigE interfaces, an optimized x16 decimator for data reduction in high-channel-count applications, and an enhanced waveform generator engine for outputting D/A data supplied by the 100 GigE interface or from waveforms loaded to on-board memory. In each case, the installed functions can provide a final solution or be the basis of a custom solution when built upon using Pentek's Navigator™ FPGA Design Kit (FDK) (see **Figure 9**).

The Navigator FDK provides a library of all of Pentek's IP functions as blocks that can be used in Xilinx's Vivado IP Integrator, giving the IP designer immediate access to the product's entire FPGA design as a block diagram. Individual IP blocks can be removed, modified, or replaced with custom IP to meet the application's processing requirements. If at any time a designer needs to work with the VHDL source code directly, it is always accessible in a source window, as well as full on-line documentation of every Pentek IP core. Navigator FDK leverages the features of Vivado, allowing an engineer to start designing with the FDK immediately without the need to learn new software tools and streamlines the path to a final application solution by providing the foundation for custom IP to be built on.

The companion product to Pentek's Navigator FDK is the Navigator Board Support Package (BSP). With every ➢

Figure 9. Pentek's Navigator FDK allows FPGA engineers to access the board design in the IP Integrator

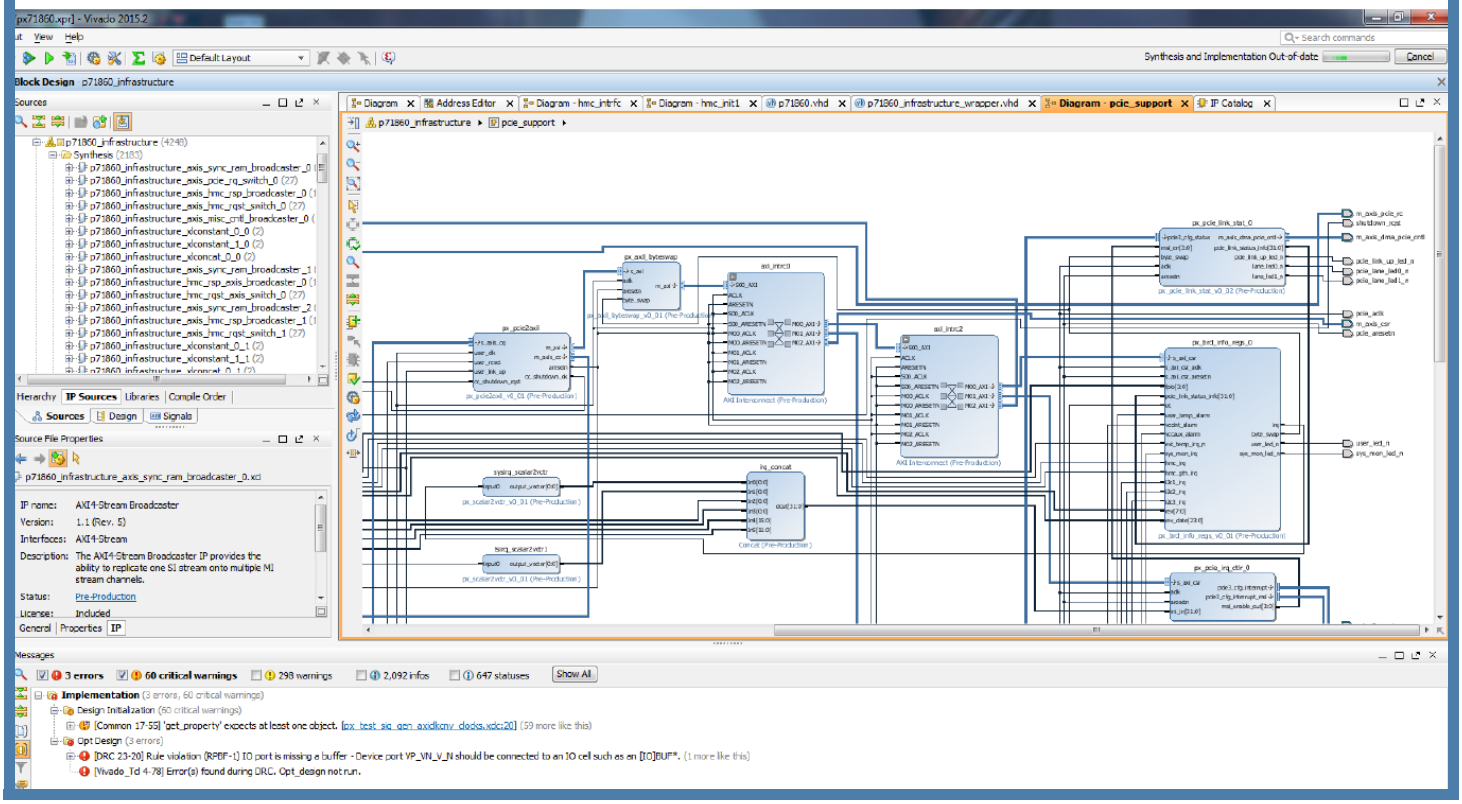
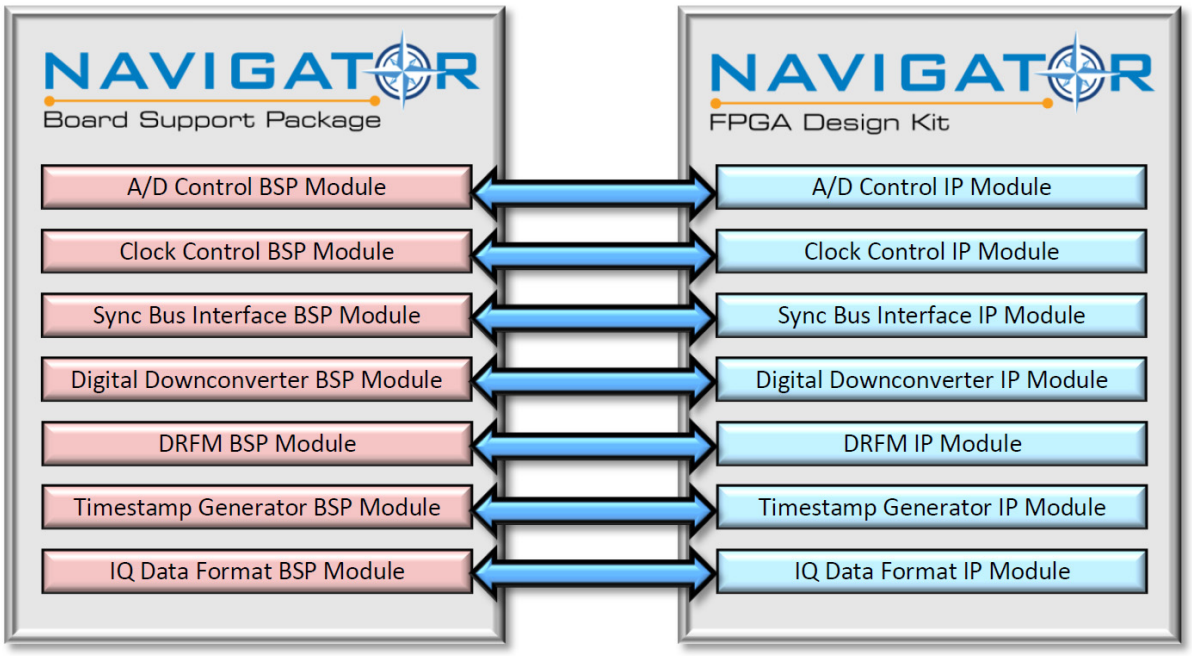


Figure 10. Navigator's one-to-one relationship between BSP modules and IP modules simplifies the task of keeping software changes synchronized with IP changes



creation of, or modification to an IP block, a change to software, most likely running on the RFSoC's ARM processors, to control the new or modified IP, might be needed. The Navigator BSP was designed to help manage this relationship between IP and software. The BSP provides C language functions and utilities structured to map the IP blocks provided in the FDK. This one-to-one relationship between IP and the software to control it is another path to manage the increasing complexity of applications (see **Figure 10**).

RFSoC brings new possibilities for addressing some of the most challenging requirements of high-bandwidth, high-channel-count systems. Understanding how this new technology can specifically address SWaP-C and low latency applications is key to matching it to many applications that can benefit from it the most. And while Xilinx has provided a rich set of tools, IP, and support at the chip level, equipment manufacturers like Pentek, using RFSoC at the center of their board architecture, can leverage the power of RFSoC by providing unique solutions to streamline the path from RFSoC to a deployed system solution. ❐

Product Focus

Model 5950

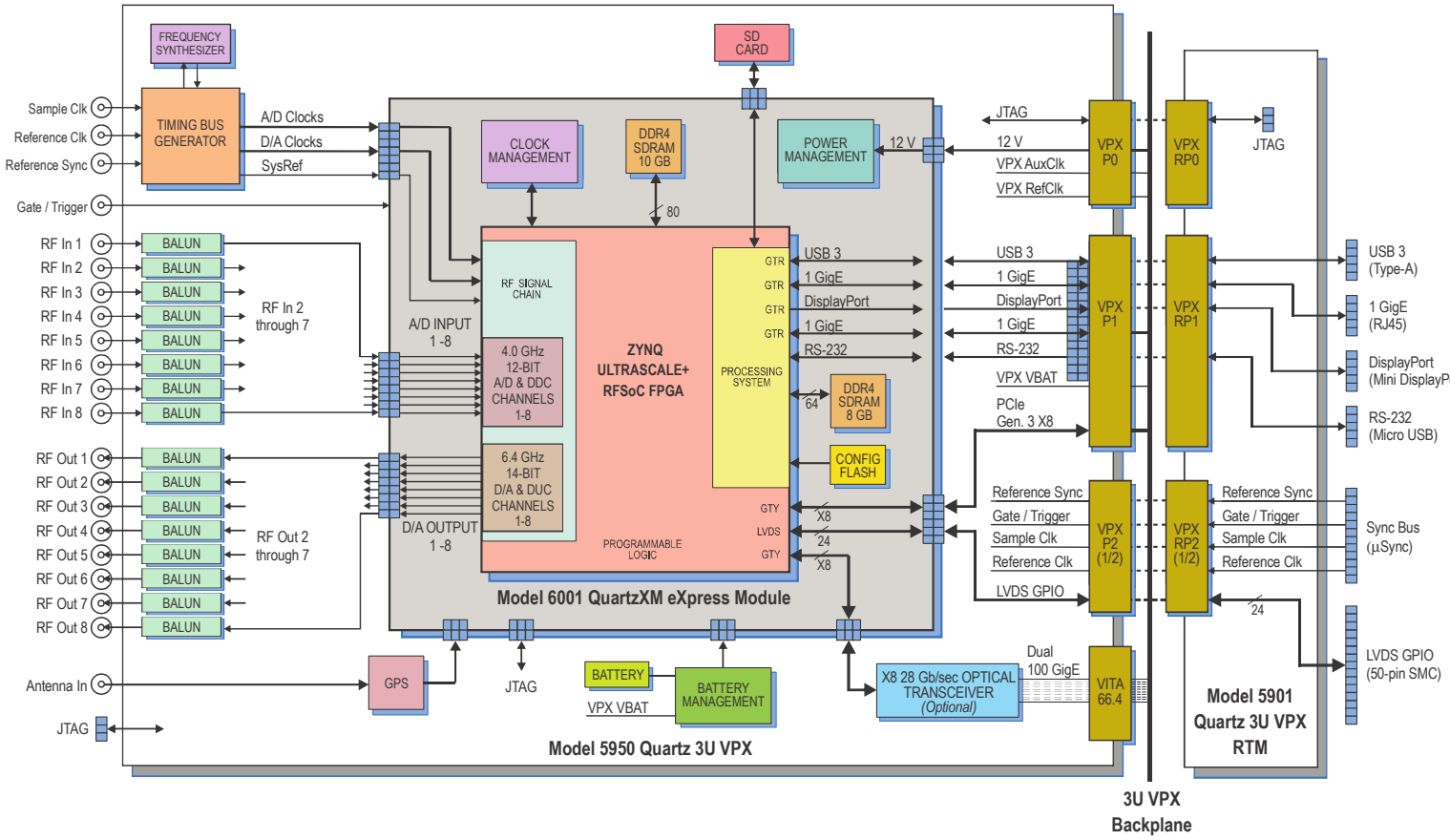
New RFSoC Board Delivers Unprecedented Resource Integration and Connectivity for Waveform Generation, Real-Time Data Acquisition, and More

QUARTZ

Pentek recently announced **Model 5950**, its first product in the **Quartz™ Architecture family**: an 8-channel A/D & D/A converter, 3U OpenVPX board based on the Xilinx Zynq UltraScale+ RFSoC FPGA (see **Figure 8**). Model 5950 offers low latency benefits that were previously not possible with earlier generation products.

"The Quartz architecture takes our board designs to a new level," said Bob Sgandurra, director of Product Management of Pentek. *"The architecture is based on our Model 6001 QuartzXM™ RFSoC eXpress Module containing the RFSoC FPGA and all needed support circuitry* (see **Figure 7**). *By addressing some of the most demanding circuit and PCB design challenges in the module, Pentek, as well as our customers, can leverage the design and use the module on a carrier in a standard form factor like 3U VPX as well as custom carriers to match specific application requirements. Customers can develop their system software and IP on the 3U VPX product in the lab and then deploy the QuartzXM Module wherever it is needed."*

"The Zynq Ultrascale+ RFSoC FPGA from Xilinx is a very high density solution providing built-in A/Ds, D/As, and ARM processing power plus additional DSP slices within the FPGA to build custom IP. Compared to discrete component solutions, the RFSoC FPGA is 50% lower in cost and a draws 40% less power," said David Gamba, Xilinx senior director for the Aerospace and Defense Market. He added, "*We are pleased that Pentek has developed board-level solutions that allow customers to take full advantage of the RFSoC technology. Their high-speed system connectivity, additional factory-installed IP for radar and communications, along with their unique QuartzXM modular design, all squarely target Mil-Aero market needs."* ➢



The Quartz Architecture Difference

Pentek's Quartz architecture embodies a streamlined approach to FPGA boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today. Designed to work with Pentek's Navigator Design Suite tools, the combination of Quartz and Navigator offers users an efficient path to developing and deploying FPGA software and IP for data and signal processing.

The Xilinx Zynq UltraScale+ RFSoC Processor integrates eight RF-class A/D and D/A converters into the Zynq FPGA fabric and quad ARM Cortex-A53 and dual ARM Cortex-R5 processors, creating a multichannel data conversion and processing solution on a single chip. Complementing the RFSoC's on-chip resources, the Quartz board architecture adds:

- 18 GBytes of DDR4 SDRAM
- Sophisticated clocking for single-board and multi-board synchronization
- High signal integrity connectors for RF inputs and outputs
- x8 PCIe Gen 3 link
- An 8-lane, 28 Gb/sec optical interface supporting a built-in dual 100 GigE interface or customer-installed protocols
- 12 LVDS general purpose I/O pairs for specialized interfaces
- QuartzXM modular design for flexible development and deployment
- Factory-installed application IP

Factory Installed IP Advances Development

The Model 5950 is pre-loaded with a suite of Pentek IP modules to provide data capture and processing solutions for many common applications. Modules include DMA engines, DDR4 memory controller, test signal and metadata generators, data packing, and flow control.

The Model 5950 can be used out-of-the-box with the built-in functions requiring no FPGA development. The board comes pre-installed with IP for triggered radar range gate engine, wideband real-time transient capture, flexible multi-mode data acquisition, and extended decimation.

Data Conversion

Model 5950's front end accepts analog IF or RF inputs on eight front panel MMCX connectors with transformer-coupling to eight 4 GSPS 12-bit A/D converters delivering either real or complex DDC samples. With additional IP-based decimation filters, the overall DDC decimation is programmable from 2 to 128.

The eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x, 4x, and 8x. Each D/A output is transformer-coupled to a front panel MMCX connector.

Expandable I/O

The Model 5950 supports the VITA-66.4 standard, providing eight 28 Gb/sec duplex optical lanes to the backplane. With two built-in 100 GigE UDP interfaces or a user-installed serial protocol, the VITA-66.4 interface enables gigabit communications independent of the PCIe interface.

Navigator Design Suite for Streamlined IP Development

Pentek's Navigator Design Suite includes: Navigator FDK (FPGA Design Kit) for custom IP and Navigator BSP (Board Support Package) for creating host software applications.

The Navigator FDK includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite, all source code and complete documentation is included. Developers can integrate their IP along with the factory-installed functions or use the Navigator kit to replace the IP with their own. The Navigator FDK Library is AXI-4 compliant, providing a well defined interface for developing custom IP or integrating IP from other sources.

The Navigator BSP supports Xilinx's PetaLinux on the ARM processors. Users work efficiently using high-level API functions, or gain full access to the underlying libraries including source code. Pentek provides numerous examples to assist in the development of new applications.

Pre–Configured SPARK System Ready for Immediate Use

With a pre-configured SPARK® VPX development system, work can begin immediately on applications. A SPARK system is delivered ready for immediate operation with Quartz hardware and Navigator software installed. In many applications, the SPARK development system can become the final deployed application platform.

Pricing and Availability

For the latest pricing, delivery and available options, **please fill out this form** and your request will be delivered to the appropriate department. To learn more about our products or to discuss your specific application please email our sales department at sales@pentek.com, **contact your local representative**, or contact Pentek directly:

John Eklund
Sales Director
Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
USA
Tel: +1 (201) 818-5900. ❒

Product Focus

Model 71865

766-Channel Software Radio Receiver for Surveillance and Wireless Applications

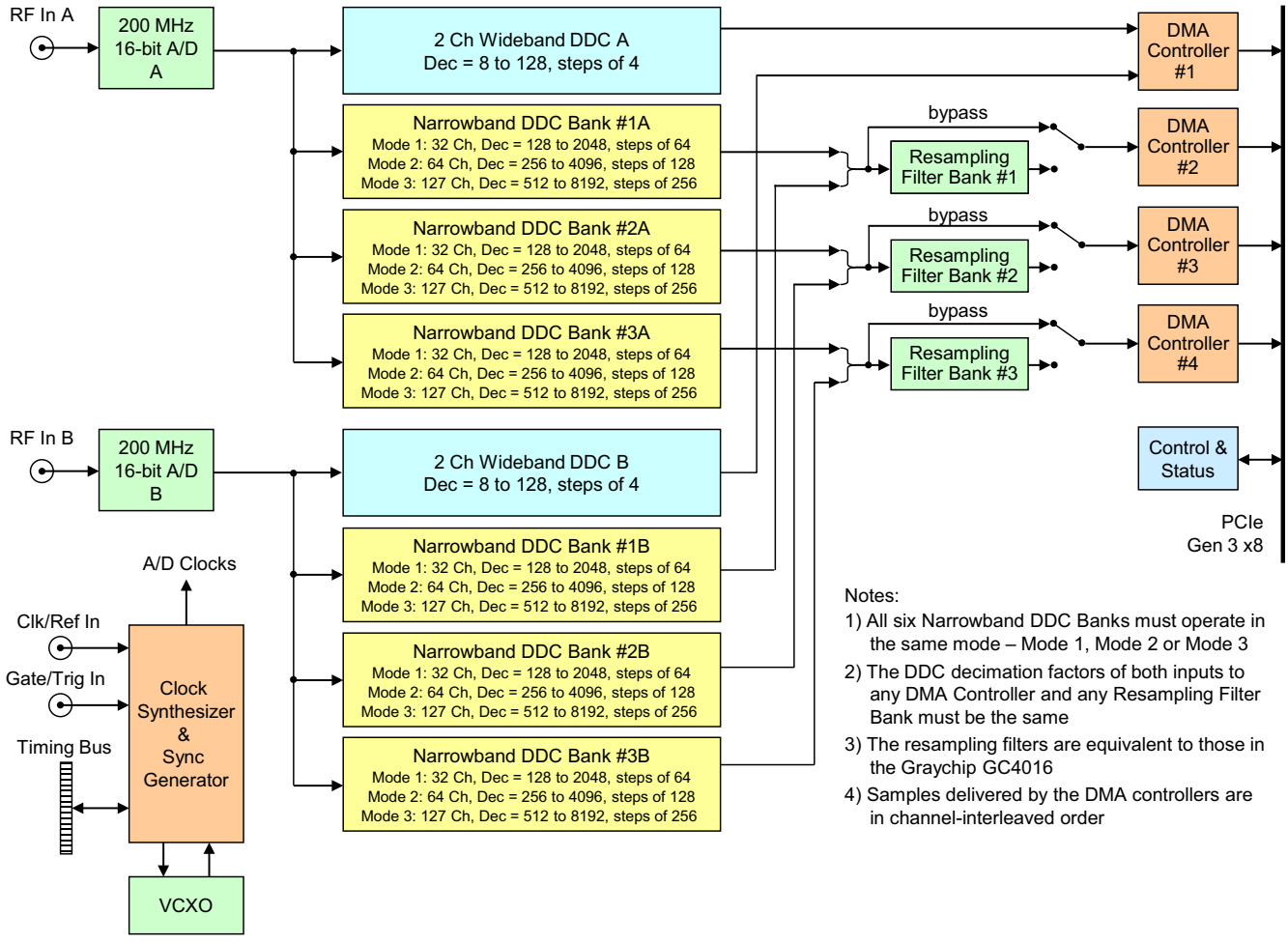
JADE

Pentek announced a new member of its highly popular Jade® family of high-speed data converter XMC FPGA modules: the 2-channel Jade Model 71865, a 200 MHz 16-bit A/D channelizer with 762 narrowband digital down converters (DDCs) and 4 wideband DDCs, based on the Xilinx Kintex UltraScale FPGA. The Model 71865 is an economical and energy efficient, complete software radio receiver solution for commercial, military and government high-channel count applications.

"Today's crowded and expensive RF spectrum is packed with a diverse variety of voice video, and data channels," said Rodger Hosking, vice-president of Pentek. *"High-density digital receivers are essential to efficiently acquire and effectively monitor these signals for quality of service, surveillance, and security applications. Emerging applications such as 5G wireless push the requirements even further."*

Factory Installed IP Advances Development

The Model 71865 functions include two A/D acquisition IP modules for simplifying data capture and transfer. Each acquisition IP module contains a powerful controller for all data clocking, triggering, and synchronization functions. From each of the two acquisition modules, A/D sample data flows into identical IP modules, consisting of banks of wideband and narrowband DDCs. Finally, data is ➢



delivered to four DMA controllers linked to the PCIe Gen.3 x8 interface for transfer to a signal processor.

DDC Resources

The four wideband DDCs can be set for decimation values between 8 and 128 in steps of 4, providing usable output bandwidths from 1.25 MHz to 20 MHz. The wideband DDCs can be quite effective in locating signals of interest.

Each of the six narrowband DDC banks can be configured to operate in three different modes, where each mode provides a different quantity of DDC channels and range of decimations. Output bandwidths range from 20 kHz to 1.25 MHz. All DDCs can be independently tuned from 0 Hz to 200 MHz with 32 bits of resolution.

Resampling Filters

Three banks of resampling filters accept input samples from each narrowband DDC at one sample rate and deliver output samples at another rate. Resampling filters are often used for better symbol recovery of signals using modern digital modulation schemes. Programmable ratios ensure flexibility to cover a wide range of wireless standards.

Navigator BSP

Pentek's Navigator BSP provides a full suite of high-level C-callable libraries that support all features of the Model 71865 and demonstrate all of its functional modes with examples. The software package is provided with complete source code, allowing the user to modify and integrate this functionality into the end application. Navigator BSP also includes an extremely useful Signal Viewer utility that allows developers to view digitized signals from the output samples of any DDC in time and frequency domain.

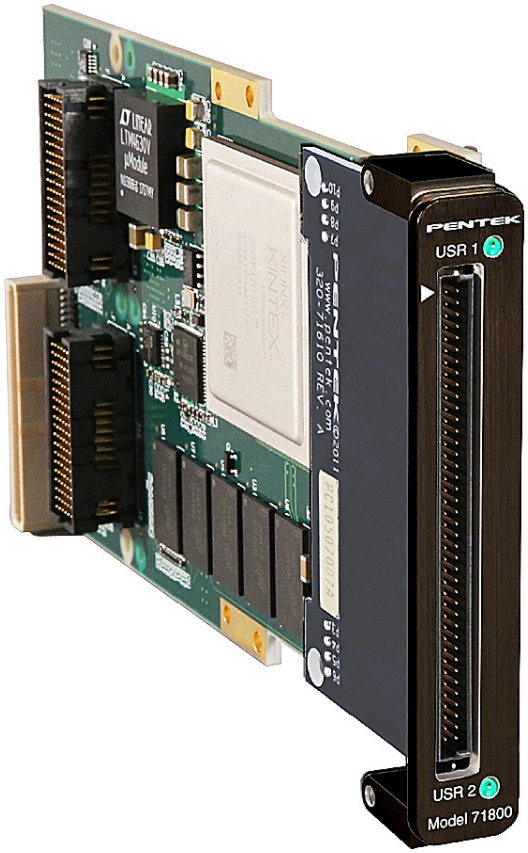
For more information, go to: https://www.pentek.com/go/pipe71865 and for the latest pricing and options, see Pricing and Availability . ❒

Kintex UltraScale Co-processor Jade XMC for Signal Processing Applications

Model 71800 is another new member of Pentek's Jade family of high-performance data converter XMC modules based on the Xilinx Kintex Ultrascale FPGA. Model 71800 is a co-processor module with an XMC PCI Express Gen 3 interface and general purpose I/O using parallel LVDS and gigabit serial ports.

The Jade Architecture embodies a streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today. Designed to work with Pentek's Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA IP for data and signal processing.

The Model 71800 is pre-loaded with IP modules for DMA engines, a DDR4 memory controller, test signal and metadata generators, data packing and flow control to speed up the development process. The 71800 is available with the Kintex UltraScale KU035, KU060 and KU115, supporting a range of processing power. The majority of the Kintex UltraScale FPGA resources are available for customer installed IP for processing and management of I/O.



Performance IP Cores

"Designers who need to boost DSP processing for an existing system, or wish to develop their own new IP application, can take good advantage of the Model 71800. Not only does it offer up to 5520 DSP slices for plenty of processing horsepower, it also provides well-defined connections to PCIe, DDR4 memory, LVDS I/O and gigabit serial links to support high-performance interfaces," said Bob Sgandurra, director of Product Management of Pentek. *"Advancements in our Navigator tools now make it much easier to integrate custom IP with modules from the Pentek library to develop solutions for very specific needs. A designer's imagination is the only limitation to the capabilities of this module."* ➢

The Jade Architecture

The Pentek Jade Architecture is based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by over 50% when compared the previous FPGA family with equally impressive reductions in cost, power dissipation and weight. As the central feature of the Jade Architecture, the FPGA has access to all data and control paths, allowing direct access to all board resources. A large 5 GB bank of DDR4 SDRAM is available to the FPGA for custom applications. The x8 PCIe Gen 3 link can sustain 6.4 GB/s data transfers to system memory. Eight additional gigabit serial lanes and 38 LVDS general purpose I/O pairs are available for specialized interfaces.

Navigator Design Suite for Streamlined IP Development

Pentek's Navigator Design Suite consists of two components: Navigator FDK (FPGA Design Kit) for integrating custom IP into Pentek designs and Navigator BSP (Board Support Package) for creating host software applications.

The Navigator FDK includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. The Navigator FDK Library is AXI-4 compliant, providing a well defined interface for developing custom IP or integrating IP from other sources.

The Navigator BSP contains high-level libraries and drivers for Windows and Linux operating systems. Users can work efficiently using high-level API functions, or gain full access to the underlying libraries including source code. Numerous examples speed development of new applications.

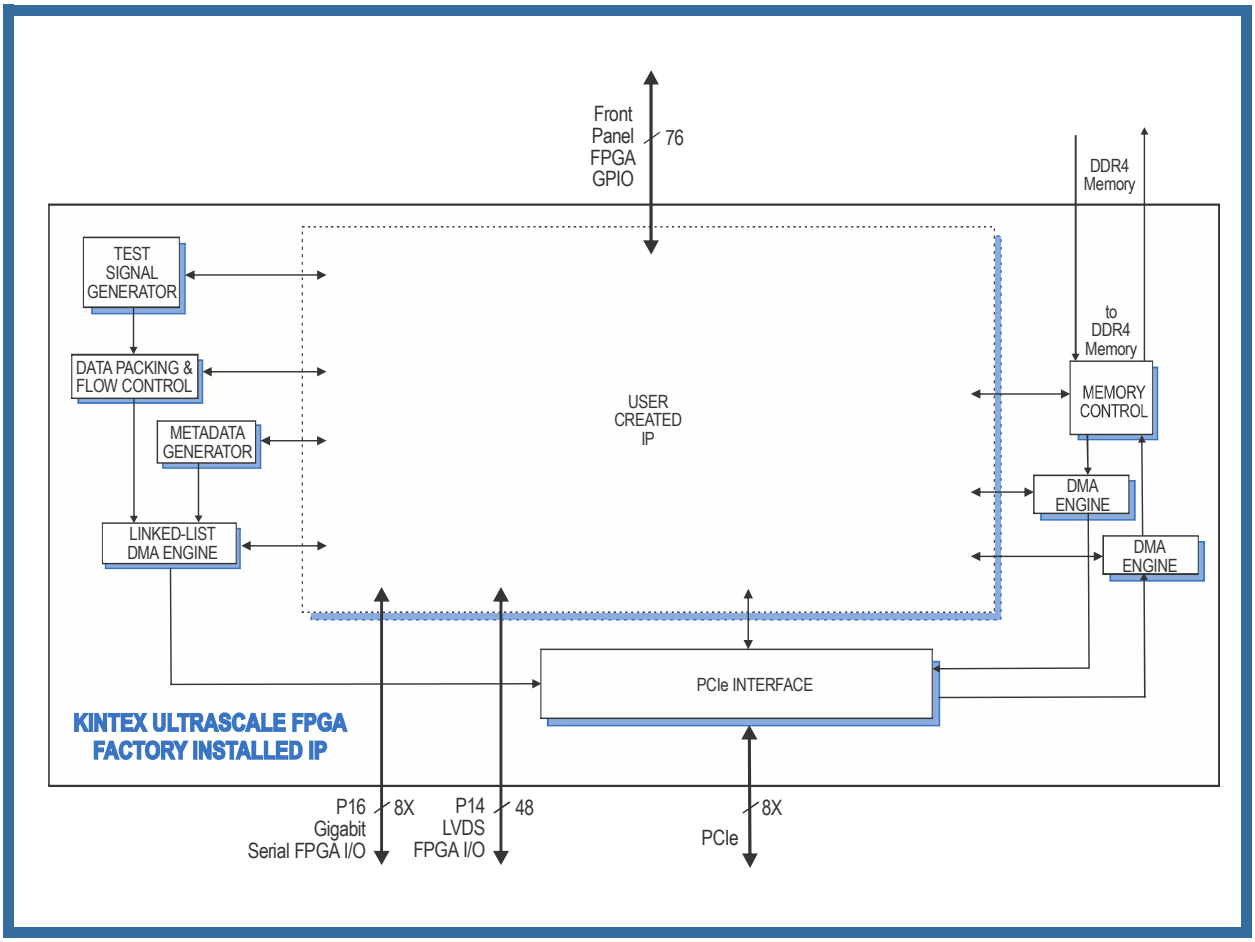
Pre–Configured SPARK Development System

With a Pentek 8266 SPARK PC, 8264 SPARK 6U VPX, or 8267 SPARK 3U VPX development system, work can begin immediately on applications. A SPARK system saves engineers time and expense associated with building and testing a development system and ensures optimum performance of Pentek boards. SPARK development systems are ready for immediate operation with software and hardware installed. In many applications, the SPARK development system can become the final deployed application platform.

Form Factors

The Model 71800 XMC module is designed to operate with a wide range of carrier boards in PCIe, 3U and 6U VPX, AMC, and 3U and 6U CompactPCI form factors, with versions for both commercial and rugged environments.

For more information, go to: https://www.pentek.com/go/pipe71800 and for the latest pricing and options, see Pricing and Availability. ❐



With Pentek's New Jade Architecture Came a New Documentation Architecture

What has changed?

- Documentation is HTML-based and can be viewed from any web browser. This new format started with the Jade family of products and will be used with Quartz and all future products.
- This new format allows easier access to the complete product documentation set (hardware, software, and IP), with all manuals linked and accessible through the same interface. A powerful search feature helps users quickly find the information they need.
- The documentation is delivered on DVD, with updates available via our FTP site, so it does not require an internet connection.

Why the change?

The **AXI4*** implementation in the Jade architecture distributes control registers throughout the block diagrams, which is different from a centralized control register memory map. Because of this, the address information must be navigated in a different way than in the past and using an HTML, linkable format puts the register information right at your fingertips.

How is it organized?

The picture below shows the user manual library for Jade Model 78851. To the left, the table of contents panel lists the HTML manuals: Getting Started, Installation, and Operation. The center of the screen provides easy access to block diagrams, memory maps, the interrupt tree, and the Navigator BSP software manual.

How do I get it?

Each Jade product is shipped with a DVD containing its user manual library. If you sign up to receive product update notifications via **YourPentek**, when the library is updated, you'll get an email notification. Clicking on the link in the email will download a short document that describes the user manual library and tells you what has been updated in it (to see an example, click here). The document also contains instructions for how to download a zip file that contains the updated library.

We are excited about this new format for our documentation because we believe it will better serve our customers. ❐

***AXI4** is the fourth generation of an interface specification from ARM® commonly used in the semiconductor industry. Xilinx has adopted this standard to create AXI4-compliant plug-and-play IP. Navigator FDK follows the AXI4 standard. For Pentek's Jade products, the FDK includes the complete IP that is factory-installed in the board. This includes all interface, processing, data formatting, DMA functions, etc. IP designers can modify or replace functions as needed to match application requirements, and will find immediate compatibility with Xilinx IP and third-party IP that uses AXI4. Designers who create their own custom IP using the AXI4 standard will find integration with the Pentek-supplied IP straightforward.