Models 7742, 7742D — Multichannel Transceiver with Virtex-4 FPGAs - x16 PCIe

Model 7742D

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Switched fabric support
- 125 MHz 14-bit A/Ds
- Digital upconverters
- 500 MHz 16-bit D/As
- Up to 1.5 GB of DDR2 SDRAM
- Xilinx Virtex-4 FPGAs
- LVDS clock/sync bus for multimodule synchronization
- Optional factory-installed IP Cores available

General Information

Model 7742 is a multichannel data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds with one upconverter and D/A converter (Model 7742), or eight A/Ds with two upconverters and D/As (Model 7742D). It attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computers.

A/D Converter Stage

The front end accepts four or eight full scale analog HF or IF transformer-coupled inputs on front panel MMCX connectors at +10 dBm into 50 ohms into Linear Technology LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into a Virtex-4 FPGA for signal processing or for routing to other module resources.

Digital Upconverter and D/A Stage

The 7742 features one or two TI DAC5686 digital upconverters (DUCs) and D/As. Each accepts a baseband real or complex data stream from its attached FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, the DAC5686 interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs up to 320 MHz to the 16-bit D/A converter. If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-4 FPGAs

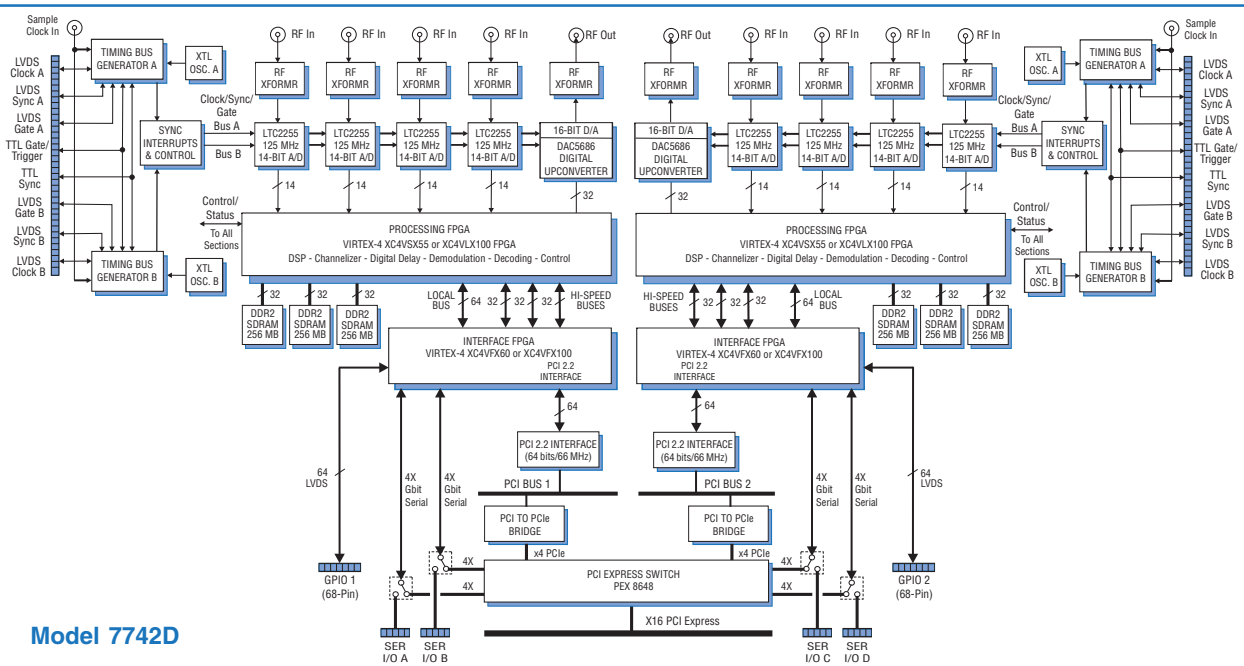
The 7742 architecture includes two (Model 7742) or four (Model 7742D) Virtex-4 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can include their own custom IP, and integrate it with factory-shipped functions using a Pentek GateFlow FPGA Design Kit.

Each Xilinx XC4VSX55 FPGA serves as a control and status engine with data and programming interfaces to each of the onboard resources including the A/D converters, DDR2 SDRAM memory, digital upconverter and D/A converter.

The XC4VSX55 features 512 DSP slices and is ideal for implementing functions such as demodulation/modulation, digital delay and channelization. For applications requiring more FPGA logic cells, these Models can be optionally configured with XC4VLX100 in place of each XC2VSX55 for up to 221,184 logic cells.

One or two Virtex-4 XC4VFX60 Interface FPGAs provide board interfaces including PCI and serial I/O. Each Interface FPGA also includes two PowerPC cores which can be used as local microcontrollers to create complete application engines. These Models can be optionally configured with XC4VFX100 in place of each FX60.

Option -104 installs a GPIO connector with 32 pairs of LVDS connections to each XC4VFX60/100 Interface FPGA for custom I/O. ➤



Model 7742D

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Multichannel Transceiver with Virtex-4 FPGAs - x16 PCIe

PCI Express Interface

The 7742 includes a multiple port, 48-lane Gen 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two optional x4 PCIe connections to each SX55/LX100 FPGA, and one x4 connection to each 64-bit PCI interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Ordering Information

Model	Description
7742	Multichannel Transceiver with four A/Ds, one D/A and Virtex-4 FPGAs - Full-length x16 PCIe
7742D	Multichannel Transceiver with eight A/Ds, two D/As and Virtex-4 FPGAs - Full-length x16 PCIe

Options:

-100	XC4VFX100 replaces XC4VFX60
-104	FPGA I/O through GPIO connector(s)
-110	XC4VLX100 replaces XC4VSX55
-428	Four multiband DDCs and interpolation filter, factory-installed core in each processing FPGA
-5xx	Gigabit Serial I/O - two full duplex 4X paths (Model 7742) or four full duplex 4X paths (7742D)

Clocking and Synchronization

Two independent internal timing buses per bank of four A/Ds can provide either a single clock or two different clock rates for the input and output signal paths.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the associated A/Ds, upconverter and D/A. Internal crystal oscillators and a front panel reference input or LVDS bus can drive the timing buses.

One or two front panel 26-pin LVDS Clock/Sync connectors allow multiple modules to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, each LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7742s can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

Three independent 256 MB banks of DDR2 SDRAM are available to each SX55 or LX100 FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and a D/A waveform generator mode. All memory banks can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +10 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 300 MHz

A/D Converters
- **Type:** Linear Technology LTC2255
- **Sampling Rate:** 1 MHz to 125 MHz
- **Internal Clock:** 125 MHz crystal osc.
- **External Clock:** 1 to 125 MHz
- **Resolution:** 14 bits
- **A/D Data Reduction Mode:** Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output
- **Output Type:** Transformer-coupled, front panel female MMCX connector
- **Full Scale Output:** +4 dBm into 50 ohms (other options available)
- **3 dB Passband:** 60 kHz to 300 MHz (other options available)

Digital Upconverter
- **Type:** TI DAC5686
- **Input Bandwidth:** 40 MHz, max.
- **Output IF:** DC to 160 MHz
- **Output Signal:** Analog, real or quadrature
- **Sampling Rate:** 320 MHz max; 500 MHz max. with upconversion disabled
- **Resolution:** 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array
- **Type:** Xilinx Virtex-4 XC4VSX55 & Xilinx Virtex-4 XC4VFX60
- **Option -100:** XC4VFX100 replaces XC4VFX60
- **Option -110:** XC4VLX100 replaces XC4VSX55

Custom I/O
- **Option -104:** Adds GPIO connector with 32 lines to each XC4VFX60/100 FPGA

Memory
- **DDR2 SDRAM:** 768 MB in three banks per SX55/LX100 FPGA (1.5 GB max.)

PCI to PCIe Interface
- **PCI Bus:** 64-bit, 66 MHz
- **DMA:** 9 channel demand-mode and chaining controller per PCI bus
- **PCIe Interface:** Gen. 2, x16 width
- **Ports:** one x4 port per PCI bus
  one x16 port to PCIe motherboard; two optional 4X ports per Interface FPGA for other gigabit protocols

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Full-length PCIe , 4.38 in. x 12.3 in.

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