New!

Models 72851 73851 and 74851

2- or 4-Channel 500 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - cPCI

Model 74851 *Model 73851*

JADE NAVIGATOR Design Suite

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two or four 500 MHz 12-bit A/Ds
- Two or four multiband DDCs (digital downconverters)
- One or two DUC (digital upconverter)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized version available

General Information

Models 72851, 73851 and 74851 are members of the Jade™ family of high-performance CompactPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71851 XMC modules mounted on a cPCI carrier board. Model 72851 is a 6U cPCI board while the Model 73851 is a 3U cPCI board; both are equipped with one Model 71851 XMC. Model 74851 is a 6U cPCI board with two XMC modules rather than one.

They include two or four A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two or four DDCs, one or two DUC, and two or four D/As. In addition to supporting PCI-X as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

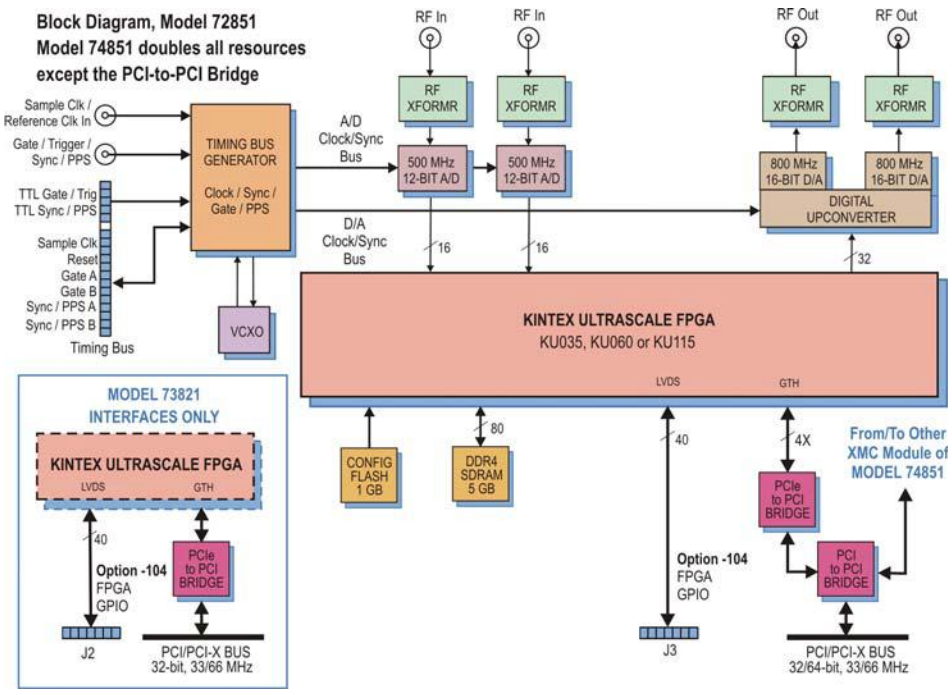
The factory-installed functions of these models include two or four A/D acquisition and two or four waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: two or four powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for data clocking and synchronization functions; test signal generators; programmable interpolators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions thereby saving the time of IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their ➤



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A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

D/A Waveform Playback IP Modules

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. They allow users to easily play back to the dual or quad D/As waveforms stored in either on-board memory or off-board host memory.

➤ own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

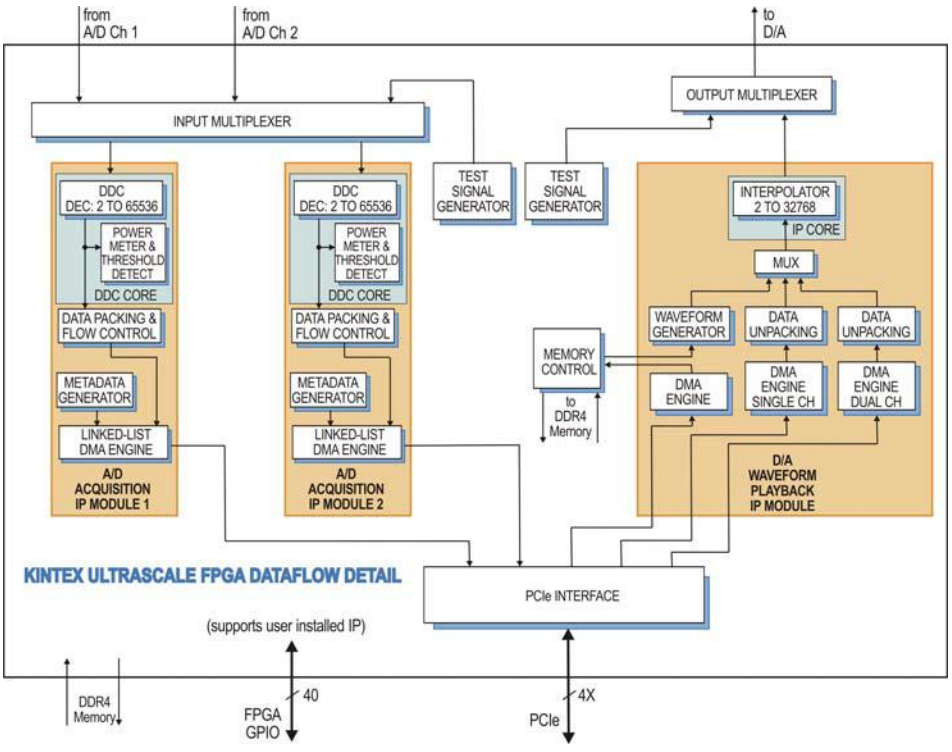
Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73851; J3 connector, Model 72851; J3 and J5 connectors, Model 74851.

A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, the Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources. ➤



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➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73851: 32 bits only. ➤

Models 72851 73851 and 74851

2- or 4-Channel 500 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - cPCI

➤ Specifications

Model72851: 2 A/Ds
Model 73851: 2 A/Ds
Model 74851: 4 A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014) (2 or 4)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters (2 or 4)
Quantity: Two channels
Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core (1 or 2)
Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73851; J3 connector, Model 72851; J3 and J5 connectors, Model 74851

Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73851: 32 bits only

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 6U Board 9.187 in x 6.717 in (233.35 mm x 170.61 mm)
3U Board 3.937 in. x 6.717 in. (100.00 mm x 170.61 mm)

Ordering Information

Model	Description
72851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U cPCI
73851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U cPCI
74851	4-Channel 500 MHz A/D with DDCs, DUC with 4-Channel 800 MHz D/A, and Kintex UltraScale FPGAs - 6U cPCI
Options:	
-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2

Contact Pentek for complete specifications of rugged version

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