New!

Models 72664, 73664 and 74664

4- or 8-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - cPCI

Model 74664 *Model 73664*

General Information

Models 72664, 73664 and 74664 are members of the Cobalt family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71664 XMC modules mounted on a cPCI carrier board.

Model 72664 is a 6U cPCI board while the Model 73664 is a 3U cPCI board; both are equipped with one Model 71664 XMC. Model 74664 is a 6U cPCI board with two XMC modules rather than one.

The output of these models supports fully the VITA-49.1 Radio Transport Standard.

These models include four or eight A/Ds, four or eight multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory- installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

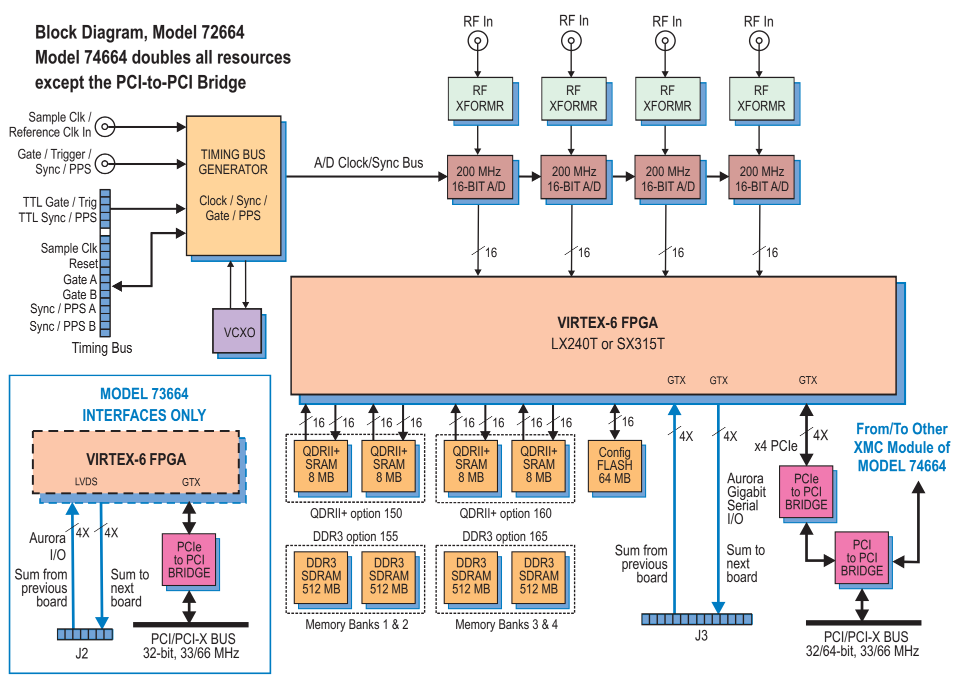
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed. ➤

Features

- Complete radar and software radio interface solutions
- Support VITA-49.1 Radio Transport Standard
- Support Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

Block Diagram, Model 72664
Model 74664 doubles all resources except the PCI-to-PCI Bridge



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A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquistion IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

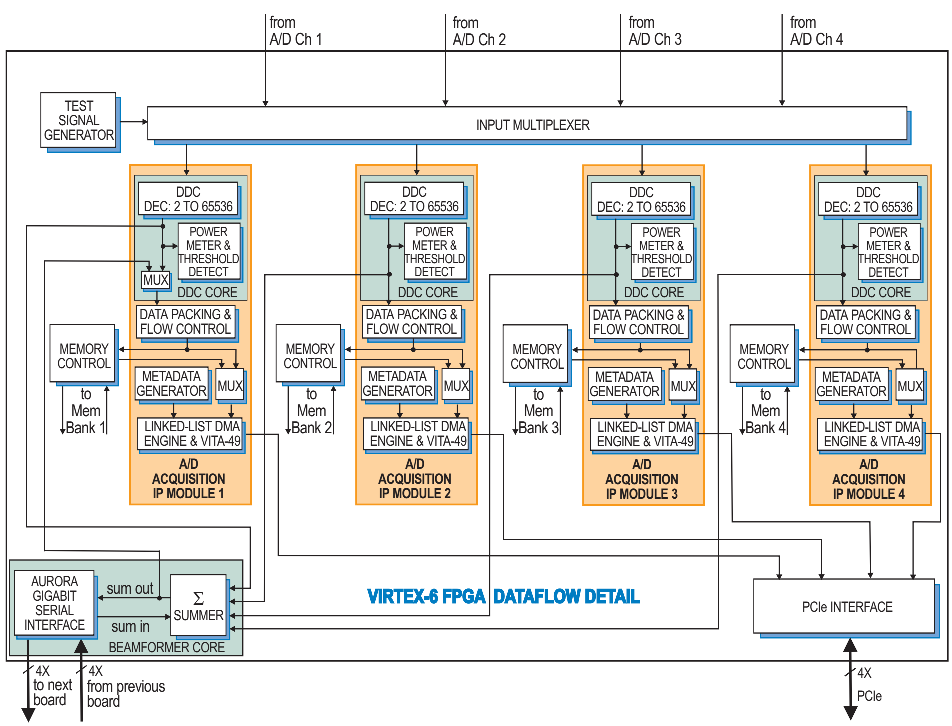
A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

➤ VITA-49

The VITA-49 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA-49 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emmisions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

These models support fully the VITA-49.1 specification. ➤



➤ A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73664: 32 bits only. ➤

Specifications

Model 72664 or Model 73664: 4 A/Ds

Model 74664: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (4 or 8)
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformers (1 or 2)
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources (1 or 2)
- On-board clock synthesizer

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Memory Banks (1 or 2)
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73664: 32 bits only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

Model	Description
72664	4-Channel 200 MHz A/D with DDCs, VITA-49, one Virtex-6 FPGA - 6U cPCI
73664	4-Channel 200 MHz A/D with DDCs, VITA-49 one Virtex-6 FPGA - 3U cPCI
74664	8-Channel 200 MHz A/D with DDCs, VITA-49, two Virtex-6 FPGAs - 6U cPCI

Options:

-062	XC6VLX240T
-064	XC6VSX315T
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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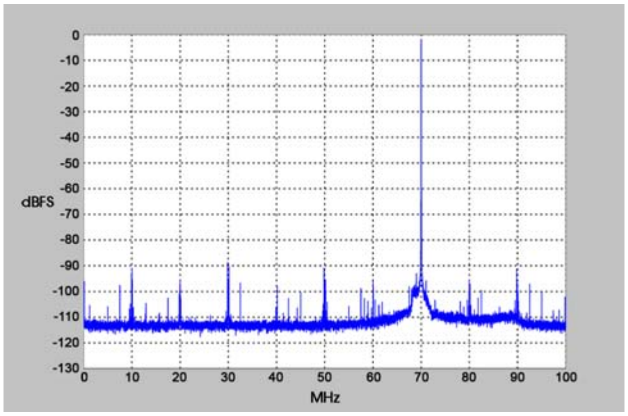
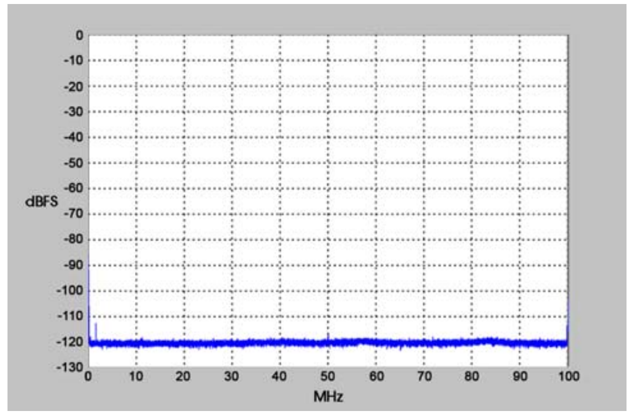
A/D Performance

Spurious Free Dynamic Range



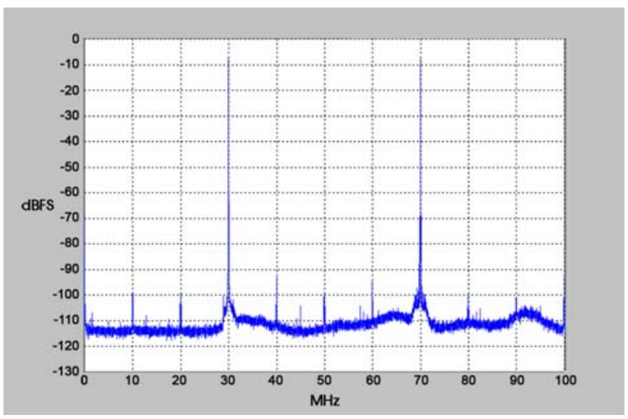
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



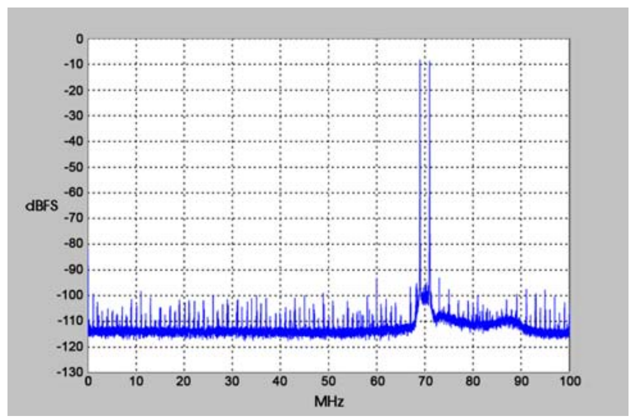
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



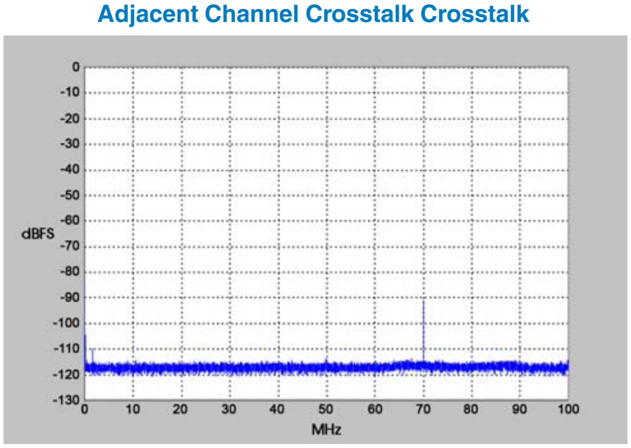
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



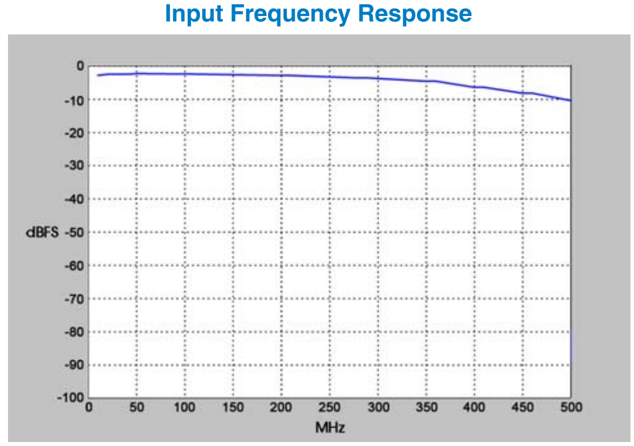
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk Crosstalk



$f_{in\ Ch2}$ = 70 MHz, f_s = 200 MHz, Ch 1 shown

Input Frequency Response



f_s = 200 MHz, Internal Clock