

New!

# Models 72132 73132 & 74132

# 8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI



Model 74132 Model 73132

## General Information

Models 72132, 73132 and 74132 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71132 XMC modules mounted on a cPCI carrier board. Model 72132 is a 6U board while Model 73132 is a 3U board; both have one Model 71132 module. Model 74132 is equipped with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections and a large DDR4 memory.

## The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container

for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

## Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

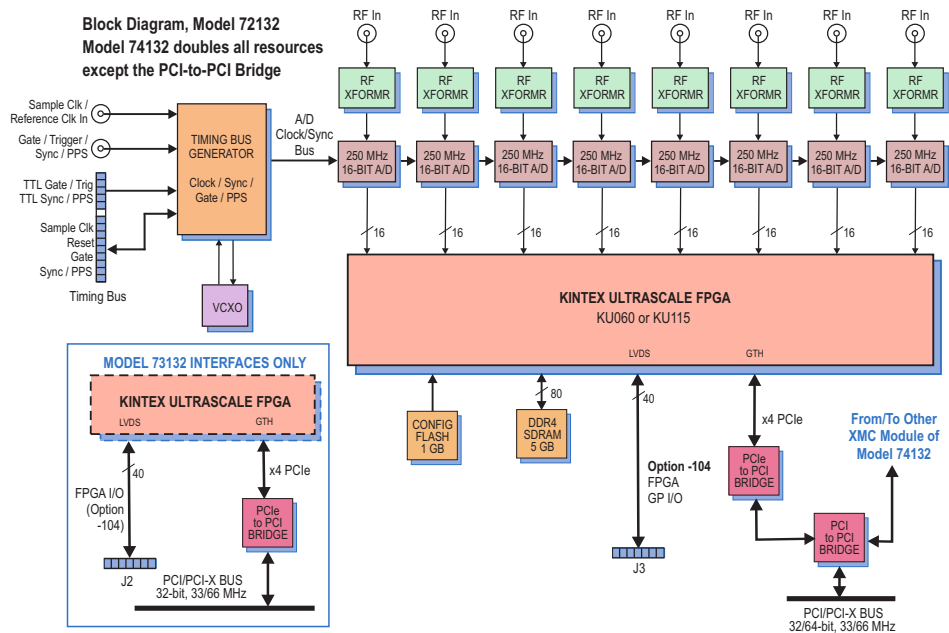
## Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ➤



## Features

- Ideal radar and software radio interface solution
- Supports one or two Xilinx Kintex UltraScale FPGAs
- Eight or 16 250 MHz 16-bit A/Ds
- Eight or 16 wideband DDCs (digital downconverters)
- 64 or 128 multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available



### A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or one or two test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

### DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The 80% default filters deliver an output bandwidth of  $0.8 \cdot f_s / N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of  $f_s / N$ .

► The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73132; J3 connector, Model 72132; J3 and J5 connectors, Model 74132.

### A/D Converter Stage

The front end accepts eight or 16 analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four or eight TI ADS42LB69 dual 250 MHz, 16-bit A/D s.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal processing or routing to other board resources.

### Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC

connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front-panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

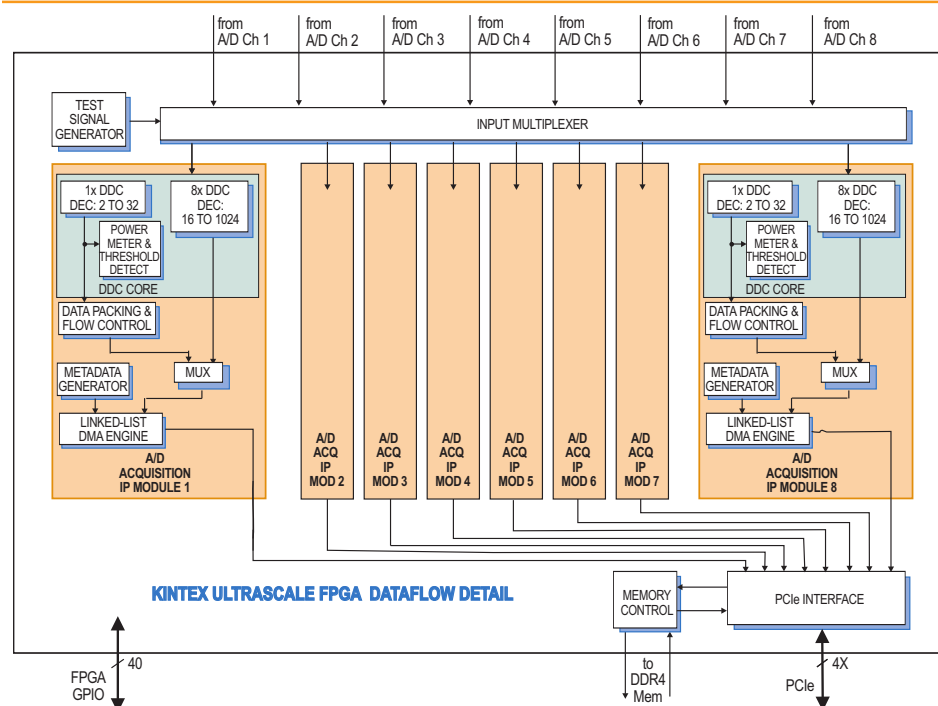
Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

### Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

### PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73132: 32 bits only. ►



► Specifications

Models 72132 and 73132: 8 A/Ds

Model 74132: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)

**Input Type:** Transformer-coupled, front panel female SSMC connectors

**Transformer Type:** Coil Craft WBC4-6TLB

**Full Scale Input:** +8 dBm into 50 ohms

**3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (8 or 16)

**Type:** Texas Instruments ADS42LB69

**Sampling Rate:** 10 MHz to 250 MHz

**Resolution:** 16 bits

Wideband Digital Downconverters (8 or 16)

**Decimation Range:** 2x to 32x

**LO Tuning Freq. Resolution:** 32 bits, 0 to  $f_s$

**LO SFDR:** >120 dB

**Phase Offset Resolution:** 32 bits, 0 to 360 degrees

**FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients

**Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters (64 or 128)

**Decimation Range:** 16x to 1024x in steps of 8

**LO Tuning Freq. Resolution:** 32 bits, 0 to  $f_s$ , independent tuning for each channel

**LO SFDR:** >120 dB

**Phase Offset Resolution:** 32 bits, 0 to 360 degrees

**FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients

**Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)

On-board clock synthesizer

Clock Synthesizer (1 or 2)

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)

**Type:** Front panel female SSMC connector, LVTTTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)

**Option -084:** Xilinx Kintex UltraScale XCKU060-2

**Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O

**Option -104:** LVDS I/O between the FPGA and J2 connector, Model 73132; J3 connector, Model 72132; J3 and J5 connectors, Model 74132

Memory

**Type:** DDR4 SDRAM

**Size:** 5 GB Models 72132 and 73132; 10 GB Model 74132

**Speed:** 1200 MHz (2400 MHz DDR)

PCI-X Interface

**PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz; Model 73132: 32 bits only

Environmental

**Standard: L0 (air cooled)**

**Operating Temp:** 0° to 50° C

**Storage Temp:** -20° to 90° C

**Relative Humidity:** 0 to 95%, non-condensing

**Option -702: L2 (air cooled)**

**Operating Temp:** -20° to 65° C

**Storage Temp:** -40° to 100° C

**Relative Humidity:** 0 to 95%, non-condensing

**Size: 6U board:** 6.299 in x 9.173 in

(160.00 mm x 233.00 mm)

**3U board:** 3.937 in x 6.299 in

(100.00 mm x 160.00 mm)

Ordering Information

Model	Description
72132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U cPCI
73132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U cPCI
74132	16-Channel 250 MHz A/D with DDCs and two Kintex UltraScale FPGAs - 6U cPCI

Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-702	Air cooled, Level L2