**Models 7241, 7241D and 7341 with Core 430**

# GateFlow Transceiver with 256/512-Ch. Narrowband DDC - cPCI

*Model 7341-430*

*Model 7241D-430*

ReadyFlow Board Support Package

GateFlow

## Features

- Complete software radio transceiver solution
- GateFlow Core 430 with 256 or 512 Channels of Narrowband Digital Downconverters factory-installed
- 256 or 512 programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256

## General Information

Models 7241-430 and 7341-430 are cPCI transceivers with 256 channels of narrowband DDCs. They consist of one Model 7141-430 transceiver mounted on a cPCI carrier board. Model 7241-430 is a 6U cPCI board, while the Model 7341-430 is a 3U cPCI board. Model 7241D-430 is the same as the Model 7241-430, except it contains two 7141-430's and doubles the number of channels to 512.

The receiver section features two LTC2255 125 MHz 14-bit A/D converters and one Texas Instruments GC4016 quad multiband digital downconverter. The GC4016 supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channel ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-Channel Digital Downconverter bank. Factory installed in the 7141-430 FPGA, Core 430 creates a flexible, very high channel count receiver system in a small footprint.

## Core 430: 256-Channel DDC Bank

Unlike legacy channelizer methods, the Pentek 430 core allows for independent programmable tuning of each channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

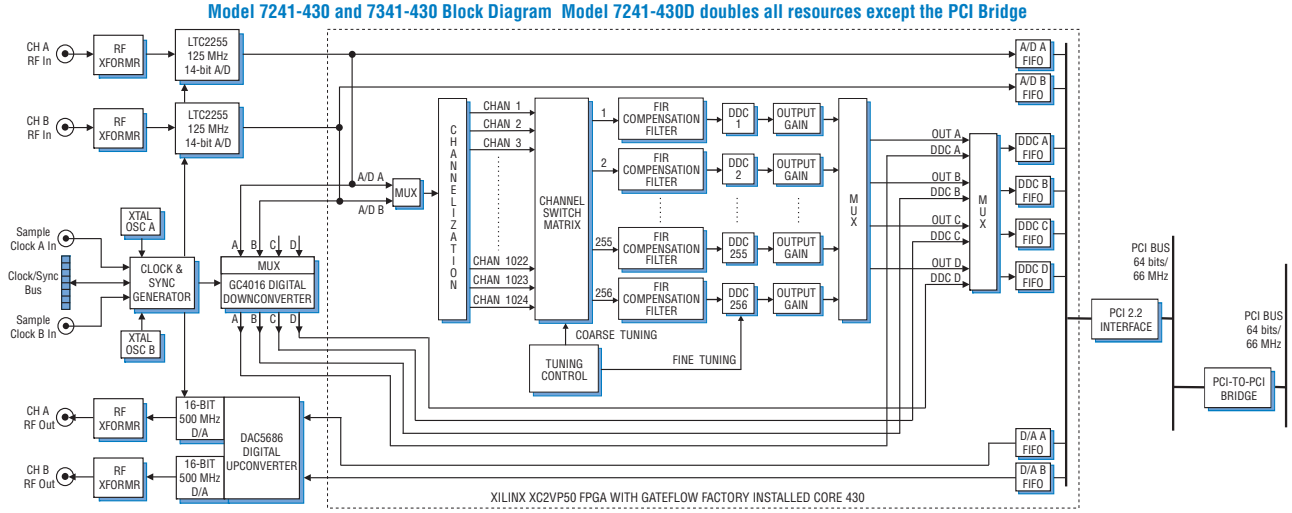
| Performance Parameter | Value |
|---|---|
| Input Data Resolution | 16-bit |
| Output Data Resolution | 16-bit Complex |
| Tuning Resolution | Clock Freq / $2^{32}$ |
| Decimation | 1024 – 9984 in steps of 256 |
| Passband Ripple | <0.4 dB with default filter coefficients |
| Usable Bandwidth | 80% with default filter coefficients |
| Stopband Attenuation | >75 dB |
| NCO SFDR | >110 dB |

## Flexible Architecture

Core 430 DDC comes factory-installed in these Models. A multiplexer in front of the core allows data to be sourced from either A/D converter, A or B. At the output, a multiplexer allows for routing either the output of the GC4016 or the Core 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any interger value between 1 and 4096. A Texas Instruments DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz. The analog outputs are transformer-coupled to front panel MMCX connectors. ➤

**Model 7241-430 and 7341-430 Block Diagram Model 7241-430D doubles all resources except the PCI Bridge**





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# GateFlow Transceiver with 256/512-Ch. Narrowband DDC - cPCI

## Ordering Information

| Model | Description |
|---|---|
| 7241-430 | GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 6U cPCI |
| 7241D-430 | GateFlow Transceiver with 512-Channel Narrowband DDC factory-installed - 6U cPCI |
| 7341-430 | GateFlow Transceiver with 256-Channel Narrowband DDC factory-installed - 3U cPCI |

*Contact Pentek for available options*

## ➤ Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7241-430's or 7341-430's, or four slave 7241D-430's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7241-430 or 7341-430 boards, or forty 7241D-430 boards may be synchronized with a Model 9190 Clock and Sync Generator.

## Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

## PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

## Specifications

**7241-430: 256-Channel DDC; 7241D-430: 512-Channel DDC; 7341-430: 256-Channel DDC**

**7241D-430 shown in the Specifications**

**Analog Signal Inputs (4)**

**Input Type:** Transformer-coupled, front panel female MMCX connectors
**Transformer Type:** Coil Craft WBC1-1TLB
**Full Scale Input:** +10 dBm into 50 ohms
**3 dB Passband:** 250 kHz to 300 MHz

**A/D Converters (4)**

**Type:** Linear Technology LTC2255
**Sampling Rate:** 1 MHz to 125 MHz
**Internal Clock:** Crystal oscillator A or B
**External Clock:** 1 to 125 MHz
**Resolution:** 14 bits

**Digital Downconverters (2)**

**Type:** TI/Graychip GC4016
**Decimation:** 32 to 16,384; with channel combining mode: 8 or 16
**Data Source:** A/D, FPGA, or PCI interface
**Control Source:** FPGA or PCI interface
**Output:** Parallel complex data

**Receiver Bypass Mode:** Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

**Front Panel Analog Signal Outputs (4)**

**Output Type:** Transformer-coupled, front panel female MMCX connectors
**Full Scale Output:** +4 dBm into 50 ohms
**3 dB Passband:** 60 kHz to 300 MHz

**Digital Upconverters (2)**

**Type:** TI DAC5686
**Input Bandwidth:** 40 MHz, max.
**Output IF:** DC to 160 MHz
**Output Signal:** Analog, real or quadrature
**Sampling Rate:** 320 MHz, max; 500 MHz max. with upconversion disabled
**Resolution:** 16 bits

**Clock Sources (4):** Selectable from onboard A or B crystal oscillators, external or LVDS clocks

**External Clocks (4)**

**Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

**Sync/Gate Bus (2):** 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

**Field Programmable Gate Array (2)**

**Type:** Xilinx Virtex-II Pro XC2VP50

**Memory**

**DDR SDRAM:** 1 GB in six banks

**PCI Interface**

**PCI Bus:** 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
**Local Bus:** 64-bit, 66 MHz
**DMA:** 9 channel demand-mode and chaining controller

**Environmental (Commercial version)**

**Operating Temp:** 0° to 50° C
**Storage Temp:** –20° to 90° C
**Relative Humidity:** 0 to 95%, non-cond.

**Size: Size:** Standard 6U cPCI board

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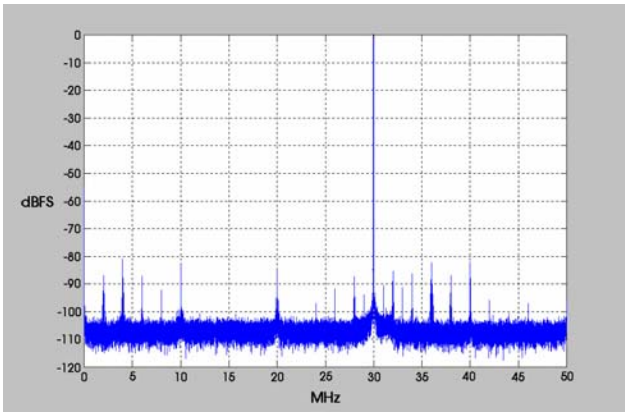
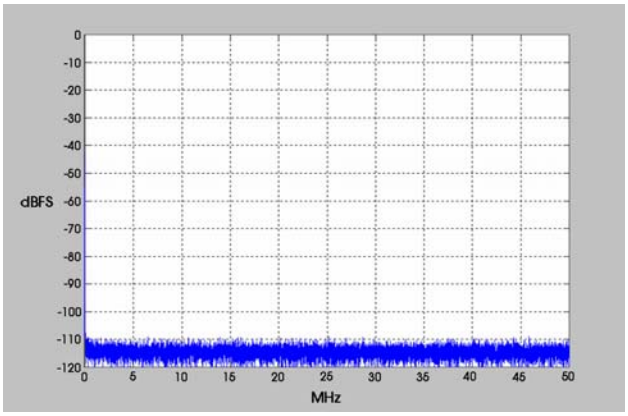
## A/D Performance

Spurious Free Dynamic Range



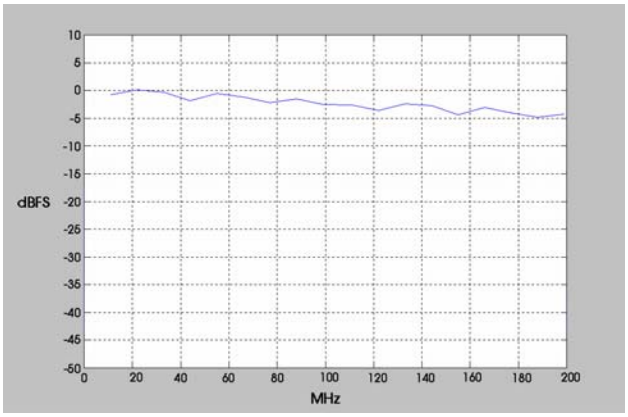

$f_{in}$ = 70 MHz, $f_s$ = 100 MHz

Spurious Pick-up



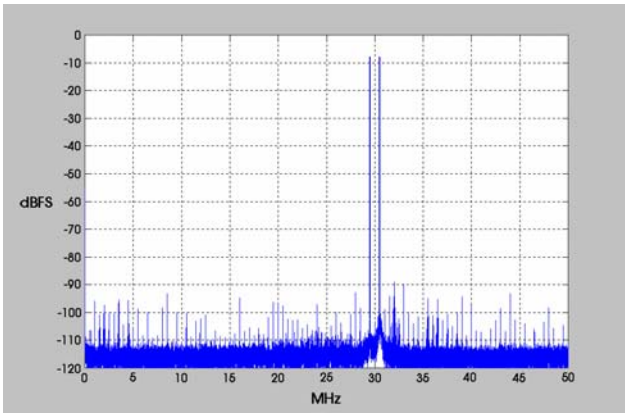

$f_s$ = 100 MHz, 32k point FFT, 8 averages

Input Frequency Response



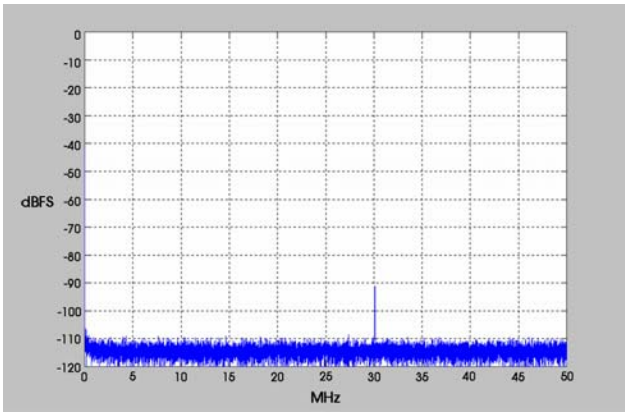

$f_s$ = 100 MHz

Two-Tone SFDR



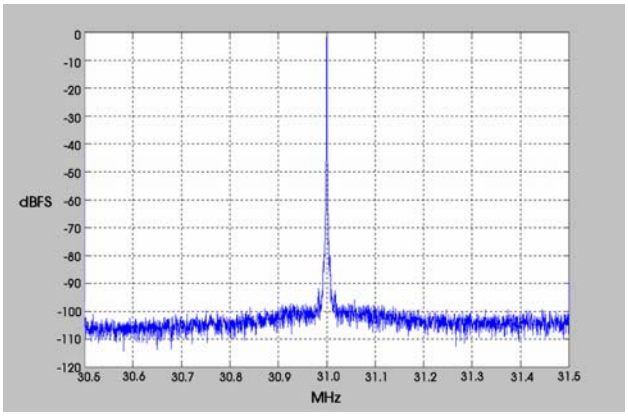

$f_1$ = 29.5 MHz, $f_2$ = 30.5 MHz, $f_s$ = 100 MHz

Crosstalk




$f_{in\ Ch2}$ = 69 MHz, $f_s$ = 100 MHz, Ch 1 shown

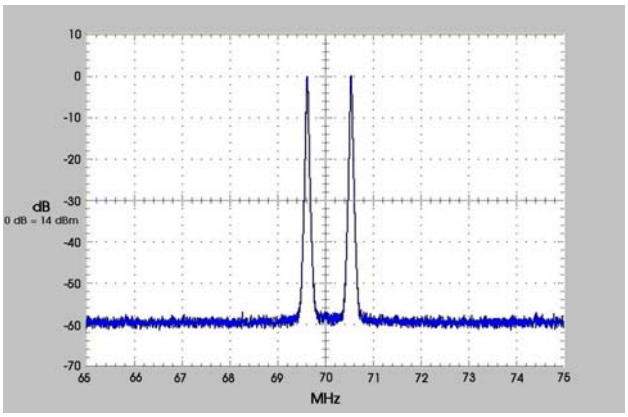
Phase Noise




$f_{in}$ = 69 MHz, $f_s$ = 100 MHz
Phase Noise @ 100 kHz = -102 - 10*log(610) = -129.8 dB/Hz

## D/A Performance

Two-Tone Intermodulation Distortion




$f_1$ = 69.5 MHz, $f_2$ = 70.5 MHz, $f_s$ = 100 MHz