Models 7240, 7240D and 7340

Dual/Quad Multiband Transceivers with FPGA - 3U/6U cPCI

Model 7340 *Model 7240D*

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio transceiver solution
- Two or four 105 MHz 14-bit A/Ds
- Input signal bandwidth up to 40 MHz
- Four or eight digital downconverters
- One or two digital upconverters
- Two or four 500 MHz 16-bit D/As
- 512 or 1024 MB DDR SDRAM
- One or two Xilinx Virtex-II Pro FPGAs
- Up to 1.28 seconds delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 or 64 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O
- Optional factory-installed IP Cores available

General Information

Models 7240 and 7340 are cPCI multiband transceivers. They consist of one Model 7140 transceiver mounted on a cPCI carrier. The Model 7240 is a 6U cPCI board, while the Model 7340 is a 3U cPCI board. Model 7240D is the same as the Model 7240, except it contains two 7140's rather than one.

A/D Converter Stage

The front end accepts full scale analog HF or IF inputs on front panel MMCX connectors at +4 dBm into 50 ohms with transformer coupling into AD6645 14-bit 105 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGAs for signal processing or for routing to other board resources.

Digital Downconverter Stages

The TI/Graychip GC4016 quad digital downconverters accept either four 14-bit inputs or three 16-bit digital inputs from the FPGAs, which determine the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the cPCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stages

The TI DAC5686 digital upconverters (DUC) and dual D/As accept baseband real or complex data streams from the FPGAs with signal bandwidths up to 40 MHz.

When operating as upconverters, they interpolate and translate real or complex baseband input signals to any IF center frequency between DC and 160 MHz. They deliver real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGAs

The Xilinx XC2VP50 Virtex-II Pro FPGAs serve as a control and status engines with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverters, digital upconverters and D/A converters.

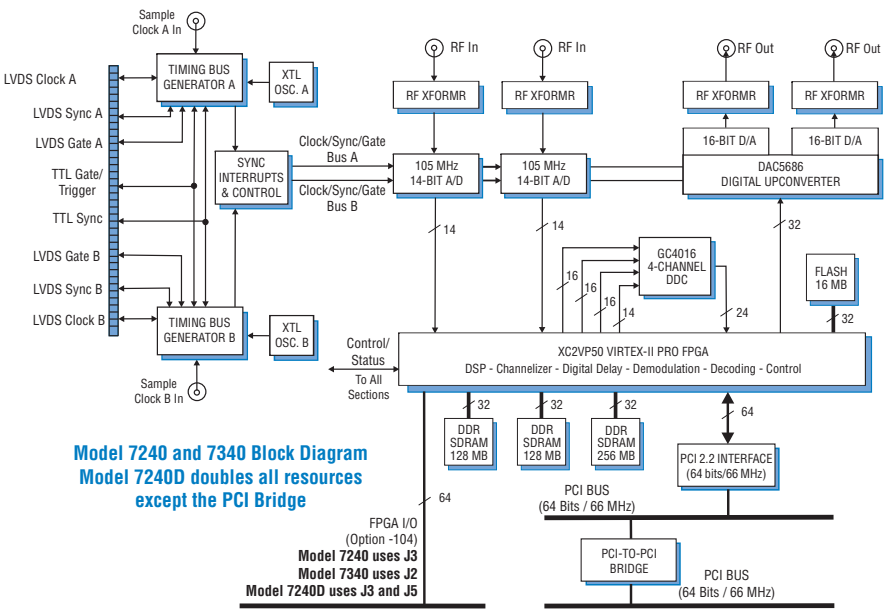
Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Option -104 adds 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O through the cPCI J3 connector. With Model 7240D, the option provides an additional 32 pairs through J5 to the second FPGA.

Each FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals. ➤



Model 7240 and 7340 Block Diagram
Model 7240D doubles all resources except the PCI Bridge

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Dual/Quad Multiband Transceivers with FPGA - 3U/6U cPCI

Ordering Information

Model	Description
7240	Dual Multiband Transceiver with FPGA - 6U cPCI
7240D	Quad Multiband Transceiver with FPGA - 6U cPCI
7340	Dual Multiband Transceiver with FPGA - 3U cPCI

Options:

-002	Full-Scale Output: –2 dBm into 50 ohms; 3 dB Passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through J3 for 7240; J2 for 7340; J3 and J5 for 7240D
-420	GateFlow Installed core: Dual wideband DDC and interpolation filter
-430	GateFlow Installed core: 256-channel narrowband DDC

Clocking and Synchronization

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7240D's or seven 7340's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7240 or 7340 boards, or forty 7240D boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

The SDRAMs are also available as a resource for the two PowerPC processor cores within each FPGA. Dual 16 MB FLASH memories support booting and program store for these processors.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7240: Dual Configuration; 7240D: Quad Configuration; 7340: Dual Configuration
7240D shown in the Specifications

Front Panel Analog Signal Inputs (4)
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Mini-Circuits ADT4-5WT
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 270 MHz

A/D Converters (4)
- **Type:** Analog Devices AD6645-105
- **Sampling Rate:** 30 MHz to 105 MHz
- **Internal Clock:** Crystal oscillator A or B
- **External Clock:** 30 to 105 MHz
- **Resolution:** 14 bits

Digital Downconverters (2)
- **Type:** TI/Graychip GC4016
- **Decimation:** 32 to 16,384; with channel combining mode: 8 or 16
- **Data Source:** A/D, FPGA, or PCI interface
- **Control Source:** FPGA or PCI interface
- **Output:** Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs (4)
- **Output Type:** Transformer-coupled, front panel female MMCX connectors
- **Full Scale Output:** +4 dBm into 50 ohms
  - **Option -002:** –2 dBm into 50 ohms
- **3 dB Passband:** 60 kHz to 300 MHz
  - **Option -002:** 400 kHz to 800 MHz

Digital Upconverters (2)
- **Type:** TI DAC5686
- **Input Bandwidth:** 40 MHz, max.
- **Output IF:** DC to 160 MHz
- **Output Signal:** Analog, real or quadrature
- **Sampling Rate:** 320 MHz, max; 500 MHz max. with upconversion disabled
- **Resolution:** 16 bits

Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks (4)
- **Type:** Front panel MMCX connectors, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array (2)
- **Type:** Xilinx Virtex-II Pro
- **Option -050:** XC2VP50
- **Option -104:** Installs J3 and J5 connectors with 64 lines to each XC2VP50 FPGA

Memory
- **DDR SDRAM:** 1 GB in six banks
- **FLASH:** 32 MB in two banks

PCI Interface
- **PCI Bus:** 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
- **Local Bus:** 64-bit, 66 MHz
- **DMA:** 9 channel demand-mode and chaining controller

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U cPCI board

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