Models 7231, 7231D and 7331

16/32-Channel Multiband Receivers with A/Ds and FPGA - cPCI

Model 7331 *Model 7231D*

GateFlow ReadyFlow Board Support Package

Features

- Two or four 80 or 105 MHz, 14-bit A/D converters
- 16 or 32 channels of multiband digital downconverters
- 5 kHz to 10 MHz output bandwidth for f_S = 100 MHz
- 250 MHz input bandwidth
- Ideal for IF sampling
- User-configurable Xilinx Virtex-II FPGAs
- Custom FPGA I/O through cPCI J2 or J3 and J5 connectors
- Bypass path allows direct capture of A/D data
- Front panel clock and sync bus
- Synchronization of up to 40 7231D or 80 7231 or 7331 with Model 9190

General Information

Models 7231 and 7342 are cPCI multichannel receivers. They consist of one Model 7131 receiver mounted on a cPCI carrier. The Model 7231 is a 6U cPCI board, while the Model 7331 is a 3U cPCI board. Model 7231D is the same as the Model 7231, except it contains two 7131's rather than one.

Front End

Models 7231 and 7331 accept analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors. Model 7231D accepts up to four analog inputs, while Model 7331 accepts two.

Each input is transformer-coupled and digitized by an AD6645 14-bit A/D converter. The AD6645 operates at a maximum sampling rate of 80 MHz in the standard unit and up to 105 MHz for option -100.

The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, or from an external sample clock supplied through a front panel SMA connector or the front panel sync bus.

Digital Downconverters

These models include four or eight TI/Graychip GC4016 quad multiband downconverter chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable channels capable of center frequency tuning from DC to $f_S/2$, where f_S is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from two of the A/D converters. A crossbar switch in each GC4016 allows the first 16 channels to select either of the first two A/D outputs, and the second group of 16 downconverter channels (Model 7231D only) to select from the second pair of A/D outputs for flexible switching.

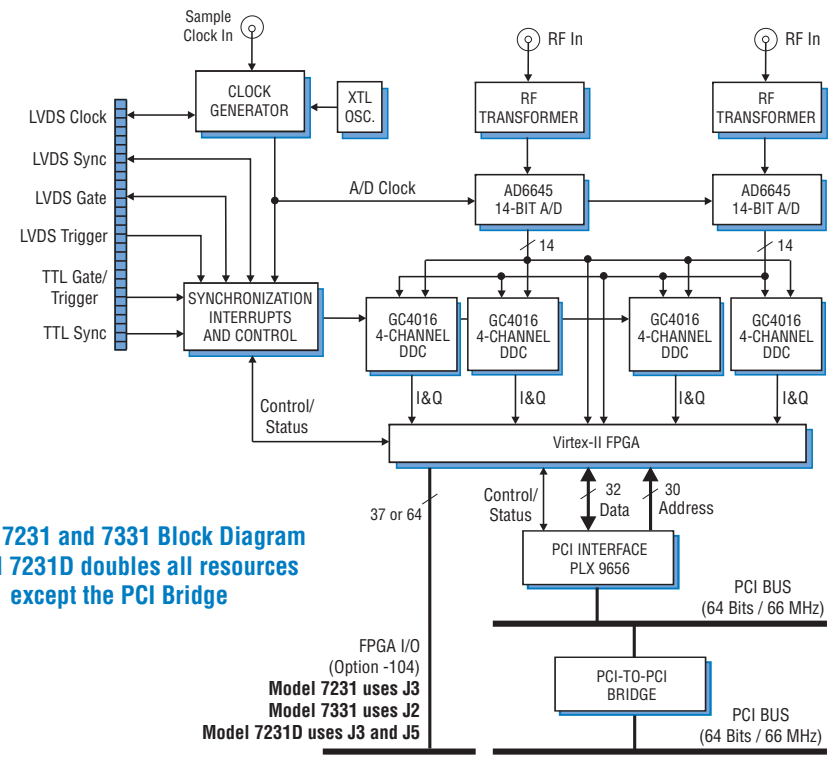
FPGA

The downconverter outputs are delivered to one or two Xilinx Virtex-II XC2V1000 FPGAs with Model 7231, or a single FPGA for Model 7331. Each FPGA is factory configured to perform various modes of data packing, formatting and channel selection, and can be upgraded to an XC2V3000.

Dual port memories in the FPGAs provide efficient PCI bus transfers by buffering downconverter and A/D data.

The A/D outputs are also connected directly to the FPGAs so that wideband A/D data can be delivered directly to the baseboard, bypassing the downconverters.

Option -104 installs the cPCI J3 connector (Model 7231) or the cPCI J2 connector (Model 7331) with 37 signal lines to the XC2V1000 or 64 lines to the XC2V3000 for custom I/O. With Model 7231D, it provides an additional 37 or 64 signal lines to the second FPGA by using the cPCI J5 connector. ➤



Model 7231 and 7331 Block Diagram
Model 7231D doubles all resources except the PCI Bridge

PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Interrupt Sources

These Models have several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload output codes, transitions on the gate signals, clock loss, buffer swapping, or a programmable over-temperature condition or faulty power supply voltage. The ADM1024 Voltage/Temperature Monitor provides constant monitoring of critical voltages and temperatures and generates an interrupt if values exceed threshold limits which are user programmable over the PCI interface.

Ordering Information

Model	Description
7231	16-Channel Multiband Receiver with A/Ds and FPGA - 6U cPCI
7231D	32-Channel Multiband Receiver with A/Ds and FPGAs - 6U cPCI
7331	16-Channel Multiband Receiver with A/Ds and FPFA - 3U cPCI
Options:	
-100	105 MHz A/D with 100 MHz oscillator
-104	FPGA I/O through cPCI J3 for 7231; cPCI J2 for 7331; cPCI J3 and J5 for 7231D
-300	XC2V3000 FPGA replaces XC2V1000

➤ Output Bandwidth

With a 100 MHz sample clock, the usable output bandwidth of each downconverter channel is 2.5 MHz. However, since these Models deliver parallel digital outputs from the GC4016 into the FPGA(s), users can take advantage of the GC4016 channel combining mode to join two or four channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.

Since each A/D converter connects directly to the FPGA(s), signals with even wider bandwidths can be accommodated.

Synchronization

The front panel clock and sync bus allow one of these Models to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple boards.

Up to four slave 7231D or seven 7231 or 7331 boards can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Using a Pentek Model 9190 Clock and Sync Generator, up to eighty 7331 or 7231 boards or up to forty 7231D boards may be synchronized. In addition to the LVDS timing bus, the Model 7231D can receive up to four TTL front panel input signals: one set of external sync and gate or trigger for the first 16 channels and one set for the second group of 16 channels.

PCI Interface

The FPGA outputs are connected to one (Model 7231 and 7331) or two (Model 7231D) 66 MHz, 64-bit PCI interfaces capable of 528 MB/sec peak data rates. Industry standard PLX9656 PCI interface chips ensure full conformance to all PCI bus timing specifications. A PCI bridge connects the two PCI interfaces to the cPCI backplane for the Model 7231D.

Specifications

Models 7231 and 7331: 16-Channel Configuration
Model 7231D: 32-Channel Configuration
Model 7231D shown in the Specifications
Front Panel Analog Signal Inputs (4)
Input Type: Transformer-coupled, front panel female SMA connectors
Transformer Type: Mini-Circuits ADT4-6T
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 270 MHz
A/D Converters, Standard (4)
Type: Analog Devices AD6645-80
Sampling Rate: 30 MHz to 80 MHz
Internal Clock: 80 MHz crystal osc.
External Clock: 30 to 80 MHz
Resolution: 14 bits
A/D Converters, Option -100 (4)
Type: Analog Devices AD6645-105
Sampling Rate: 30 MHz to 105 MHz
Internal Clock: 100 MHz crystal osc.
External Clock: 30 to 105 MHz
Resolution: 14 bits
Clock Source (2): Onboard crystal oscillator, front panel ext clock, or LVDS clock
External Clock (2): Front panel female SMA connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms impedance
Sync/Gate Bus (2)
Type: 26-pin connector, with one clock, one sync, and two gate input/output LVDS signals; two trigger LVDS inputs; and one sync and one gate input TTL signals
Digital Downconverters (8)
Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D outputs are connected to all GC4016's
Output: Parallel complex data
Bypass Mode: Data from the A/D converters can be written directly into the FPGAs at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096
Field Programmable Gate Array (2)
Type: Xilinx Virtex-II XC2V1000 standard
Option -300: Virtex-II XC2V3000
Option -104: Installs J3 and J5 connectors with 37 lines to each XC2V1000 or 64 lines to each XC2V3000 FPGA
Dual Port RAM Data Buffers
Quantity: 2 per FPGA
Size: 4k x 32 DPRAM expandable to 8k x 32 with option -300 FPGA
PCI Interface
Type: PLX Technology PCI 9656
PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
Local Bus (FPGA): 32-bit, 66 MHz
Data Transfer Modes: Direct slave mode and DMA mode
PCI Bridge: 64-bit, 66 MHz
Environmental:
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U cPCI board