Model 71610

LVDS Digital I/O with Virtex-6 FPGA - XMC

General Information

Model 71610 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 71610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's interface. The 71610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

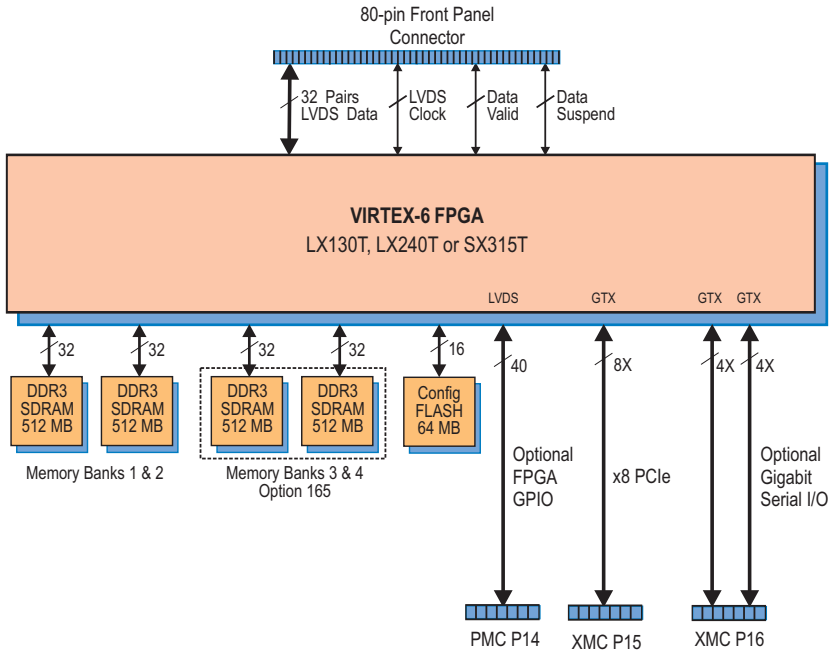
The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O to the carrier board.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board



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Model 71610 LVDS Digital I/O with Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
Model	**Description**
71610	LVDS Digital I/O with Virtex-6 FPGA - XMC
Options:	
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ Acquisition IP Module

The module can be configured for digital input mode by setting a jumper on the board. In this case, the module accepts input data Clock and input Data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The module can optionally generate a Data Suspend output signal indicating that the 71610 is no longer capable of accepting data. The module accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

Generation IP Module

The module can be configured for digital output mode by setting a jumper on the board. In this case, the module generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The module can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

XMC Interface

The Model 71610 complies with the VITA 42.0 XMC specification. Each of two connectors provides multilane gigabit serial interfaces with up to a 6 GHz bit clock. With dual XMC connectors, the 71610 supports x4 or x8 PCIe on the primary P15 XMC connector. The secondary P16 XMC connector is used for dual 4X or single 8X user-installed gigabit serial interfaces, such as Aurora, PCIe and serial RapidIO.

PCI Express Interface

The Model 71610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Memory Resources

The 71610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM

Specifications

Front Panel Input/Output

Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant

Clock: One LVDS differential pair, 2.5 V compliant

Data Valid: One LVDS differential pair, 2.5 V compliant

Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR

Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: –20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

PENTEK

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