



**Features**

- One or two 10-bit, 2 GHz A/D converters
- Xilinx Virtex-II Pro FPGA
- Dual 4X full duplex VXS links
- Two or four front panel FPDP or FPDP II outputs
- Up to 1 GB DDR SDRAM
- Multiboard synchronization: up to eight dual-channel 6826's may be synchronized with the Model 6890 clock, sync and gate distribution board
- *Ruggedized and conduction-cooled versions available*

**General Information**

The Model 6826 is a high-frequency single or dual channel A/D converter in a 6U VMEbus form factor. It accepts one or two front panel analog inputs and delivers digital output samples over two or four FPDP connectors utilizing FPDP or FPDP II standards. The 6826 is an ideal high-speed data acquisition front end for real-time recorders, digital receivers and DSP systems.

**Input Stage and A/D Converter**

The 6826 features one or two Atmel AT84AS008 2 GHz, 10-bit A/D converters driven from single-ended transformer- or DC-coupled RF signals applied through front panel MMCX female connectors at -2 dBm full-scale into 50 ohms. Although the standard transformer-coupled input circuitry accepts signals to 1 GHz, higher frequency input options are also available.

An innovative dual-stage demultiplexer packs groups of eight data samples into 80-bit words for delivery to the FPGA at one eighth the sampling frequency ( $f_s/8$ ). This advanced circuit features the Atmel AT84CS001 Demultiplexer that represents a significant improvement over previous technology.

**Clocking, Gating and Triggering**

The A/D converter sample clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz. This clock is accepted through a front panel MMCX connector with 50 ohm termination and distributed to both A/D converters (dual-channel version).

Synchronization and triggering circuitry supports synchronous data acquisition across multiple boards. Additional front panel MMCX connectors are provided for the

application of an  $f_s/8$  clock to support multi-board synchronization.

**Virtex-II Pro FPGA**

The 6826 utilizes a Model XC2VP70 Xilinx Virtex-II Pro FPGA. The FPGA is equipped with 512 MB of DDR SDRAM (optionally expandable to 1 GB) and 16 MB of FLASH memory.

Several data packing modes allow formatting output data across multiple FPDP ports. The FPGA also acts as a controller for board functions such as gate/trigger. Optional LVDS I/O is available through either the VMEbus P2 connector or a second-slot front panel mezzanine.

**FIFOs and FPDP Outputs**

Following the FPGA, two or four 32-bit wide FIFO buffers with a depth of 32k words are useful as elastic memory to support hard disk latencies in recording applications.

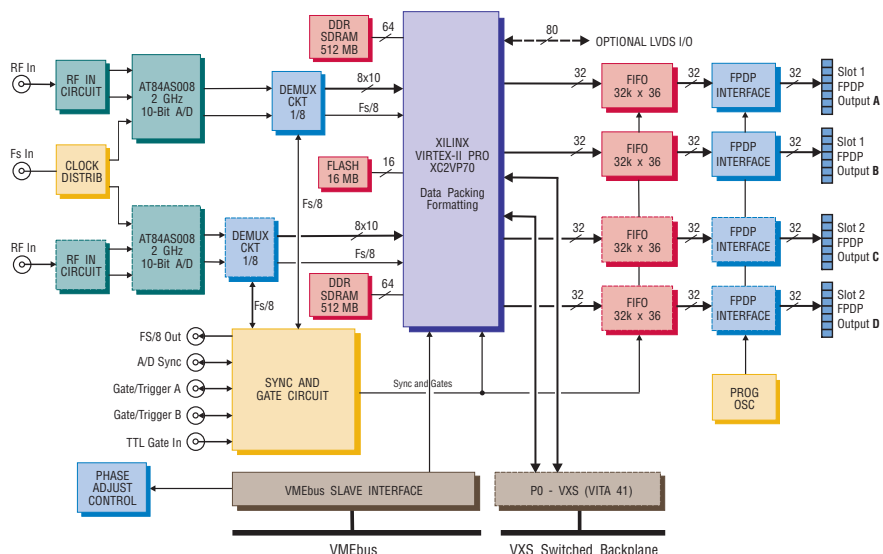
A total of four FPDP output ports are available, each supporting data transfers of up to 400 MB/sec. Two FPDP ports are attached to the 6826 front panel; optionally, two additional ports attach to a second slot front panel (not available in conduction-cooled units).

**Optional VXS Interface**

The 6826 provides two optional 4X full duplex VITA-41 links to the VXS P0 connector, each capable of peak rates to 1.25 GB/sec. These links support Gigabit fabrics such as Xilinx Aurora, Serial RapidIO and PCI Express.

**Switchless VXS Card Cage**

A five-slot card cage with full fabric support for three payload cards without the need for a switch card is available for developing and testing VXS cards. ➤



## ► Specifications

### Front Panel Analog Signal Inputs

**Quantity:** 1 or 2

**Input Type:** Transformer-coupled, front panel female MMCX connectors

**Full Scale Input:** -2 dBm into 50 ohms

**Transformer 1 dB Passband:** 50 MHz to 1 GHz

### A/D Converters

**Quantity:** 1 or 2

**Type:** Atmel AT84AS008

**Sampling Rate:** 200 MHz to 2 GHz

**Internal Clock:** None

**External Clock:** 200 MHz to 2 GHz

**Resolution:** 10 bits

**Bandwidth:** 3.3 GHz at full power

### Digital Demultiplexer Circuit

**Quantity:** 1 or 2

**Overall Demux Ratio:** 1:8

**Initial Stage:**

**Type:** Atmel AT84CS001

**Demux Ratio:** 1:4

**Tunable Delay:** -250 ps to +250 ps

**Programmability:** User-programmable

**Output Resolution:** 10 bits

**Secondary Stage:**

**Type:** Xilinx XC2VP4 FPGA

**Demux Ratio:** 1:2

**Output Resolution:** 10 bits

**Clock Source:** Front panel external clock

**External Clock:** Front panel female MMCX connector, sine wave, 0 to -2 dBm, AC coupled, 50 ohms impedance

**A/D Sync Input/Output:** Front panel female MMCX connector, low voltage PECL

**Gate/Trigger Control:** One or two front panel female MMCX connectors, low voltage PECL; one female MMCX connector, TTL

### Field Programmable Gate Array

**Quantity:** 1

**Type:**

**Option -070:** Virtex-II Pro XC2VP70-6 FPGA I/O:

**Option -121:** Provides forty LVDS differential data I/O pairs, two clock I/O pairs and four control pairs from the FPGA to VMEbus P2 connector

**Option -222:** Adds two 68-pin connectors through a second-slot front panel; each provides twenty LVDS data I/O differential pairs, one LVDS clock I/O pair and two control I/O pairs

### Memory

#### DDR SDRAM:

**Quantity:** Two banks

**Size:** 256 MB per bank, 512 MB total standard; 512 MB per bank, 1 GB total with option -340

**Bus Width:** 64 bits

**Speed:** 125 MHz; 250 MHz double data rate

### FLASH:

**Quantity:** 1

**Size:** 16 MB

**Bus Width:** 16 bits

### Front Panel Data Port (FPDP) Outputs

**Quantity:** 2 standard; 4 with option

-224 (additional ports located on second slot front panel)

**Output Type:** non-inverted configuration, FPDP I or FPDP II

**Clock:** Onboard programmable oscillator (up to 50 MHz)

### FIFOs

**Quantity:** 2 standard, 4 with option -224

**Size:** 32,768 x 36

**Speed:** 133 MHz

### VME Slave Interface

**Type:** Slave A16/D16, A16/D32, A24/D24 (A32/D32 programmable)

**Control:** Operating modes, gate/trigger, FIFO reset, data packing, FPDP I/II selection, status

### Power

**Default Configuration:** 50 W (one A/D) to 60 W (dual A/D)

User FPGA designs will increase power consumption within the following ranges:

**With XC2VP70 FPGA:** from 50 W to 75 W typical

### Environmental (Commercial version)

**Pentek Ruggedization Level:** L0

**Cooling Method:** Forced air

**Operating Temp:** 0 to 50° C

**Storage Temp:** -20 to 90° C

**Relative Humidity:** 0 to 95%, non-condensing

### Environmental - Option -703

**Pentek Ruggedization Level:** L3

**Cooling Method:** Conduction cooling

**Operating Temp:** -40 to 70° C

**Storage Temp:** -50 to 100° C

**Relative Humidity:** 0 to 95%, non-condensing

**Sine Vibration:** 10 g, 20-2,000 Hz

**Random Vibration:**

0.1 g<sup>2</sup>/Hz, 20-2,000 Hz

**Shock:** 30 g, 11 ms

### Environmental - Option -720

**Relative Humidity:** 0 to 100% non-condensing with conformal coating

**Size:** Standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 20.3 mm (0.8 in.) wide; Option -222 or -224: 40.6 mm (1.6 in.) wide

**Weight:** 1025 grams (2.26 lbs.)

## Ordering Information

Model	Description
6826	Dual 2 GHz, 10-bit A/D with Virtex-II Pro FPGA - VME/VXS

### Options:

-001	Single A/D Converter
-002	Dual A/D Converter
-070	XC2VP70 FPGA
-121	LVDS I/O through P2
-222	2nd Slot LVDS I/O
-224	2nd Slot FPDP I/O
-340	1 GB DDR SDRAM
-5xx	VXS Interface
-70x	Ruggedized & conduction-cooled versions