New

Models 57141 & 58141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

Model 58141

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One or two-channel mode with 6.4 GHz, 12-bit A/Ds
- Two-or four-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two or four-Channel 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Models 57141 and 58141 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71141 XMC modules mounted on a VPX carrier board. Model 57141 is a 6U board with one Model 71141 module while the Model 58141 is a 6U board with two XMC modules rather than one.

They includet two or four A/Ds, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

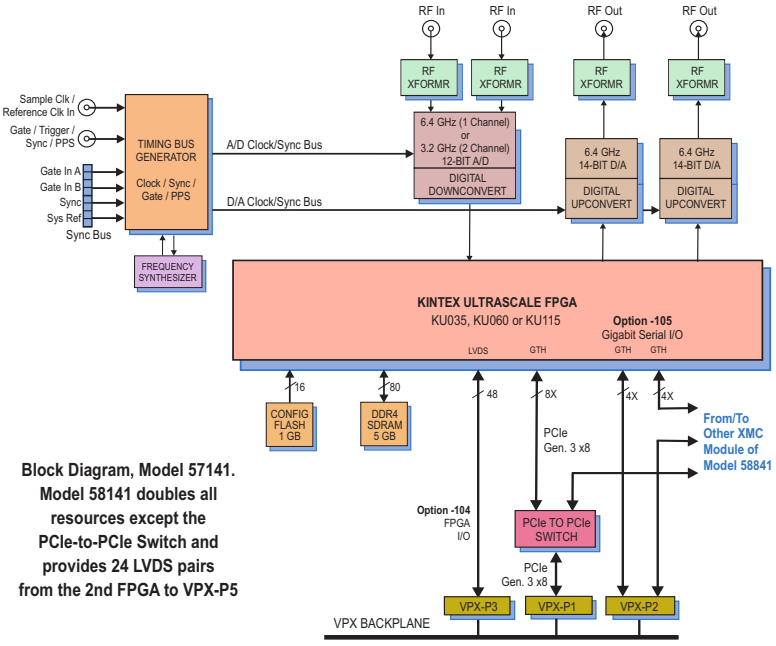
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include two or four A/D acquisition and two or four D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



Block Diagram, Model 57141. Model 58141 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

These models support factory- installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141; P3 and P5 connectors, Model 58141.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes, the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The architecture supports 5 or 10 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core(s) within the FPGA can take advantage of the memory for custom applications.

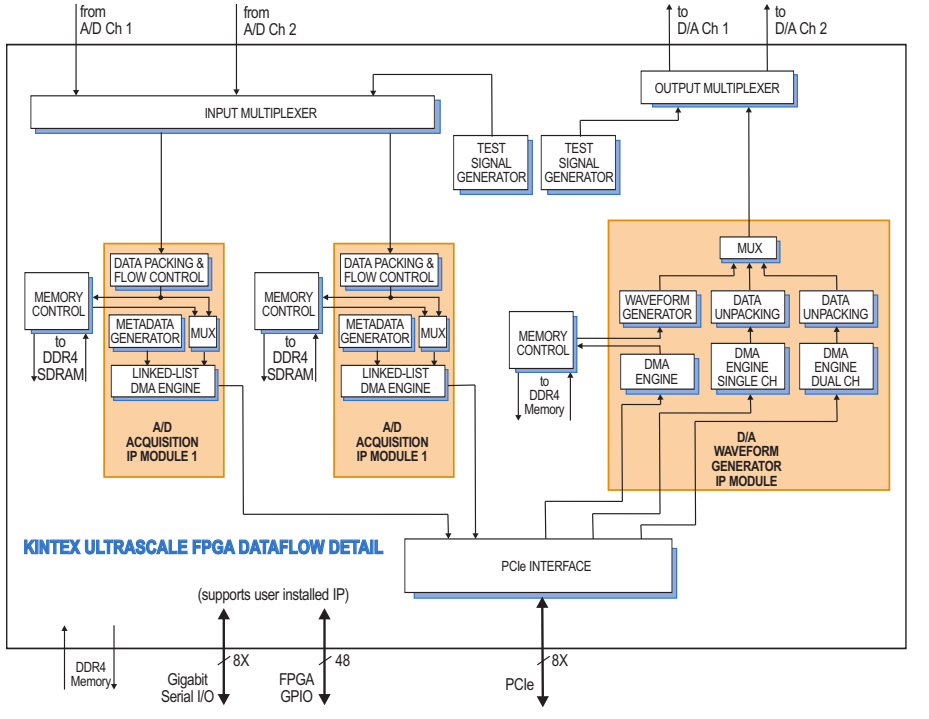
PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

These models accept a sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal ➤



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Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

➤ for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5792 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

Specifications

Model 57141 One A/D
Model 58141 Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz
D/A Converters (2 or 4)
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits
Sample Clock Source (1 or 2)
Front panel SSMC connector
Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141; P3 and P5 connectors, Model 58141.
Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.
Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 or 10 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Ordering Information

Model	Description
57141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 6U VPX
58141	2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, 4-Ch. 6.4 GHz D/A, 2 ea. Ultra-Scale FPGAs - 6U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 702	Air cooled, Level L2
- 713	Convection cooled, Level L3

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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