

New!

Model 56821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56821 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating,

triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 56821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

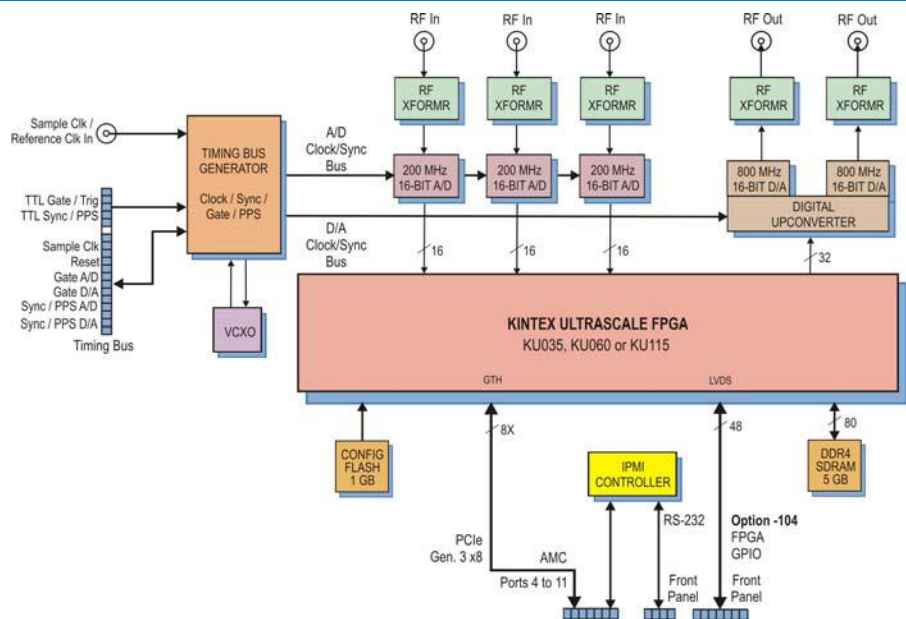
Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 56821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115. ➤



A/D Acquisition IP Modules

The 56821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

widths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

D/A Waveform Playback IP Module

The Model 56821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily playback to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

► The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

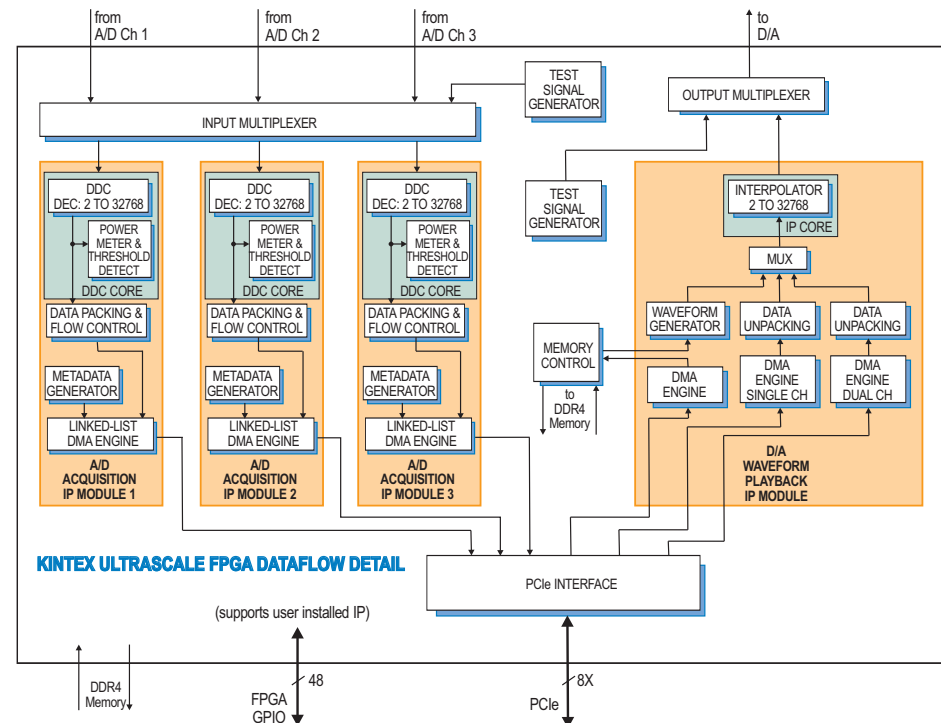
Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. ►

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output band-



► When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 56821's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

AMC Interface

The Model 56821 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or μ TCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ►

► Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters

Quantity: Two channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core

Interpolation Range: 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs

Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104 provides 24pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.60 mm)

Ordering Information

Model	Description
56821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - AMC

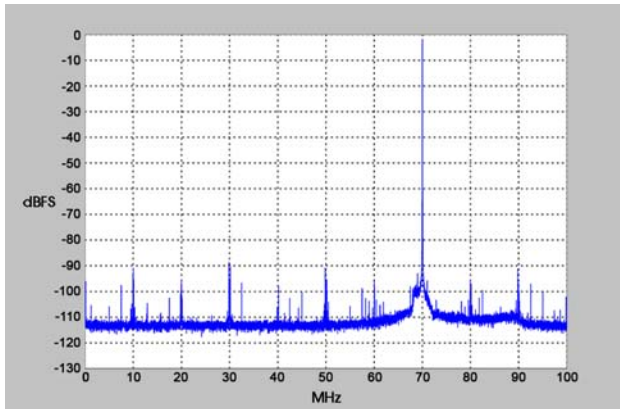
Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O to front-panel connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

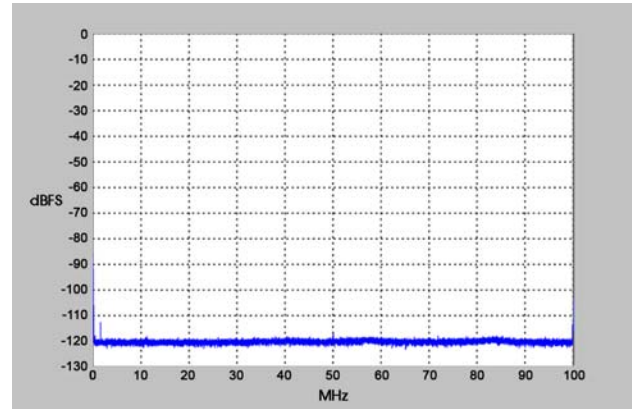
A/D Performance

Spurious Free Dynamic Range



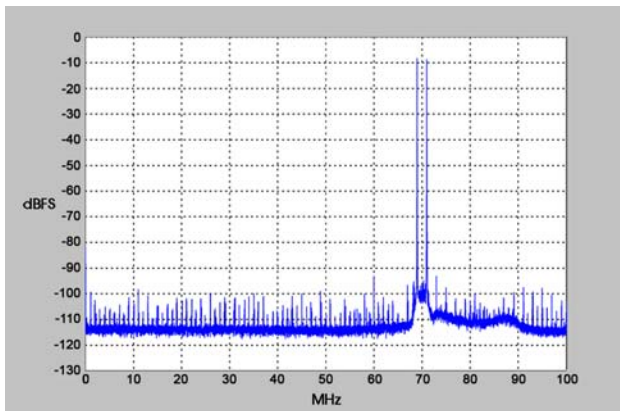
$f_{in} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

Spurious Pick-up



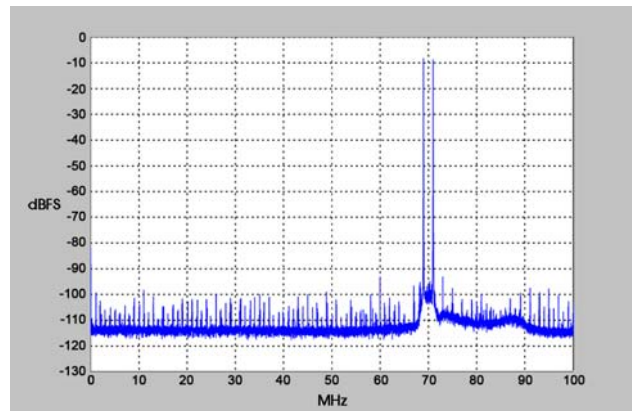
$f_s = 200 \text{ MHz}, \text{Internal Clock}$

Two-Tone SFDR



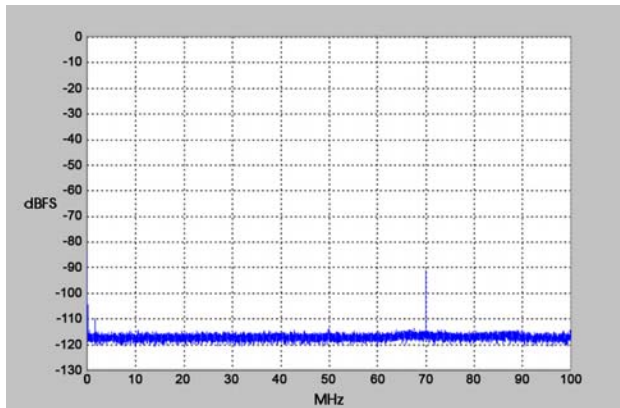
$f_1 = 30 \text{ MHz}, f_2 = 70 \text{ MHz}, f_s = 200 \text{ MHz}$

Two-Tone SFDR



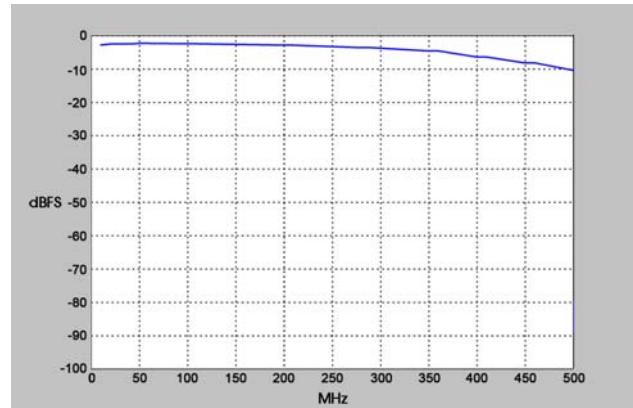
$f_1 = 69 \text{ MHz}, f_2 = 71 \text{ MHz}, f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



$f_{in \text{ Ch2}} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Ch 1 shown}$

Input Frequency Response



$f_s = 200 \text{ MHz}, \text{Internal Clock}$