New!

Model 56800

Kintex UltraScale FPGA Coprocessor- AMC

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS to the FPGA for custom I/O
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56800 is a member of the Jade™ family of high-performance AMC modules. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 56800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

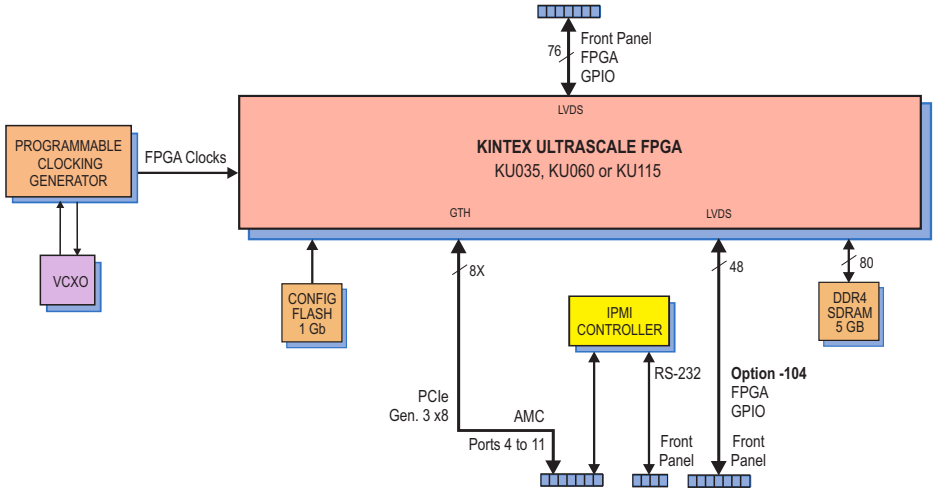
The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Front Panel Digital I/O Interface

The 56800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤



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New!

Model 56800

Kintex UltraScale FPGA Coprocessor- AMC

Memory Resources

The 56800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

➤ PCI Express Interface

The Model 56800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56862 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Digital I/O
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.6 mm)

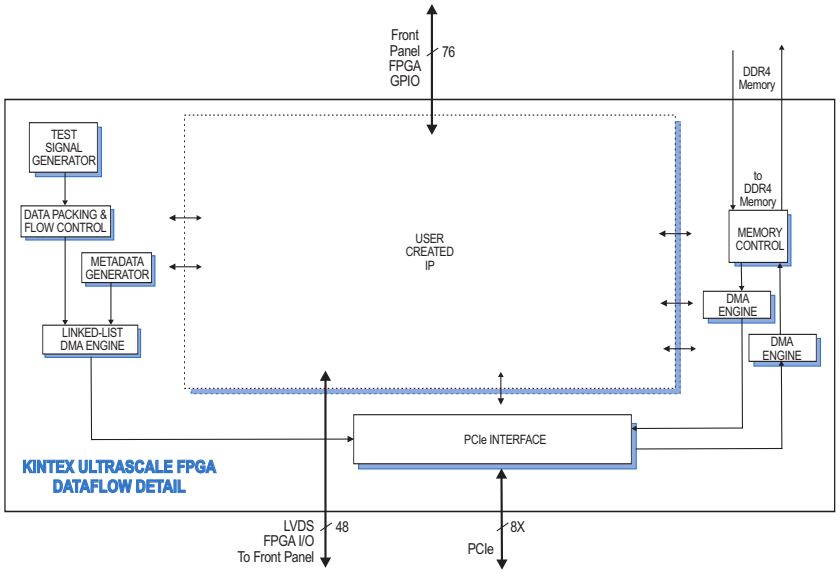
Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9

Ordering Information

Model	Description
56800	Kintex UltraScale FPGA Coprocessor - AMC
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 702	Air cooled, Level L2
- 713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions



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