

New!

Model 56132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC



Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

General Information

Model 56132 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container

for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

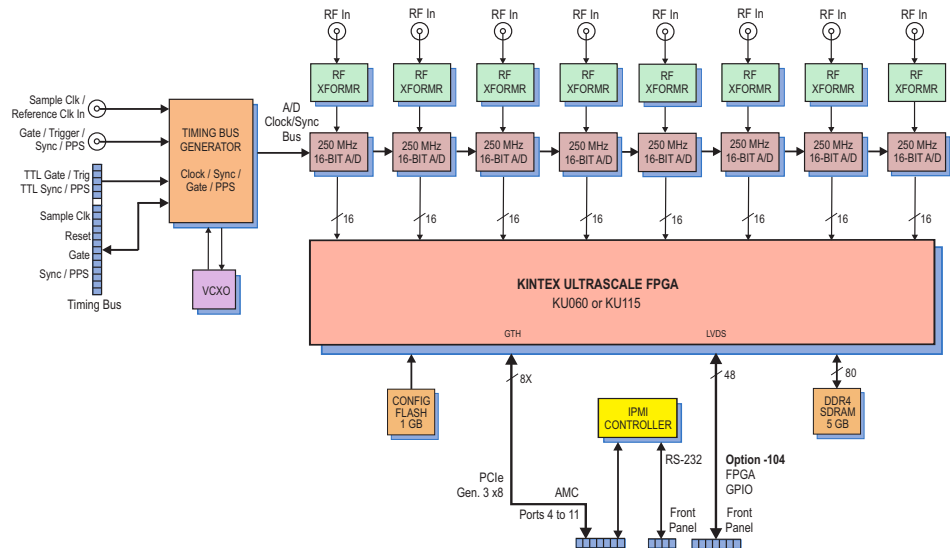
Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. ▶



A/D Acquisition IP Modules

The 566862 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

► The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

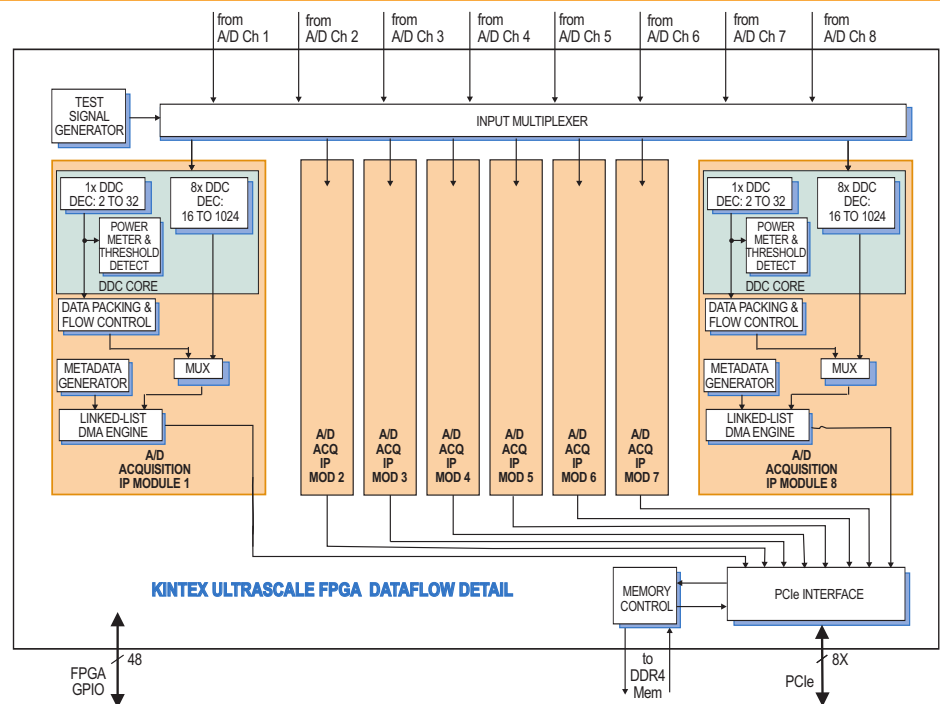
In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 5693 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications. ►



► PCI Express Interface

The Model 56132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56132 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or μ TCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Wideband Digital Downconverters

Quantity: Eight channels
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters

Quantity: Eight banks, 8 channels per bank
Decimation Range: 16x to 1024x in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to f_s , independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female MMCX connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O

Memory

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module
2.890 in x 7.110 in (73.40 mm x 180.6 mm)

Ordering Information

Model	Description
56132	8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

Options:

-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through front-panel connector
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions