New

Model 52141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Model 52141 Commercial (left) and rugged versions

JADE NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Supports VITA-49.2 VITA Radio Transport standard
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52141 is a member of the Jade™ family of high-performance PCIe modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

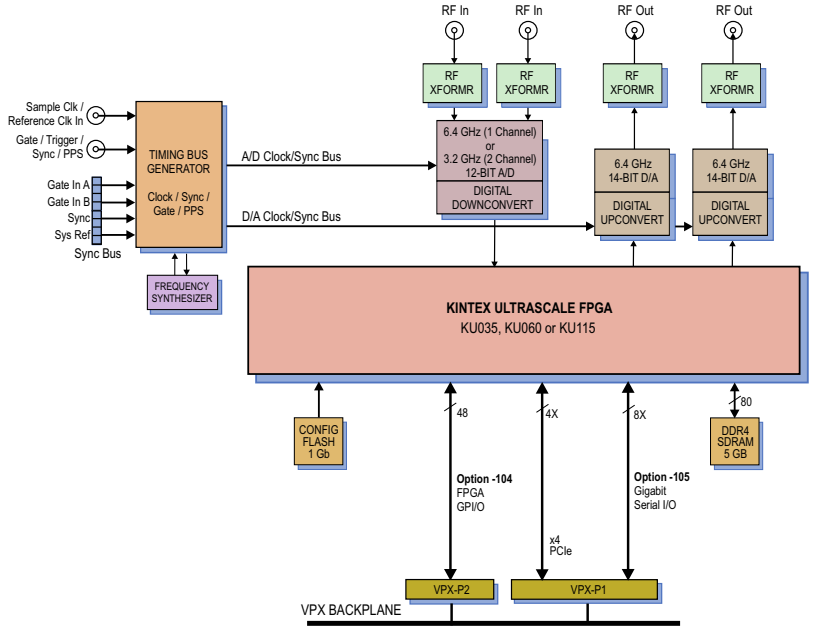
Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤



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A/D Acquisition IP Module

The 52141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 52141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

VITA 49.2 Radio Transport Standard

VITA 49.2 is a data transport protocol for conveying digitized signal information among signal acquisition/generation and processing elements in a communication, radar or similar system.

The Model 52141 implements the VITA 49 packet format for the ADC/DDC data being transferred to the host memory via DMA.

VITA 49.2 packet elements always supported are:

- Signal Data Packet Type
- Stream Identifier
- Integer Seconds Timestamp
- Fractions Seconds Timestamp
- Trailer

Programmable elements are:

- Packet Size
- Stream Identifier
- Trailer

The Timestamp is automatically inserted from the metadata engine. After initialization an externally applied 1 PPS pulse will increment the Integer Seconds Timestamp. A division of the sample clock will increment the fractional seconds timestamp and this count is reset by the 1 PPS pulse.

VITA 49 packets sent via DMA to the DAC/DUC for output will have the header, stream ID, timestamp and trailer removed leaving only the signal data to be transmitted.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

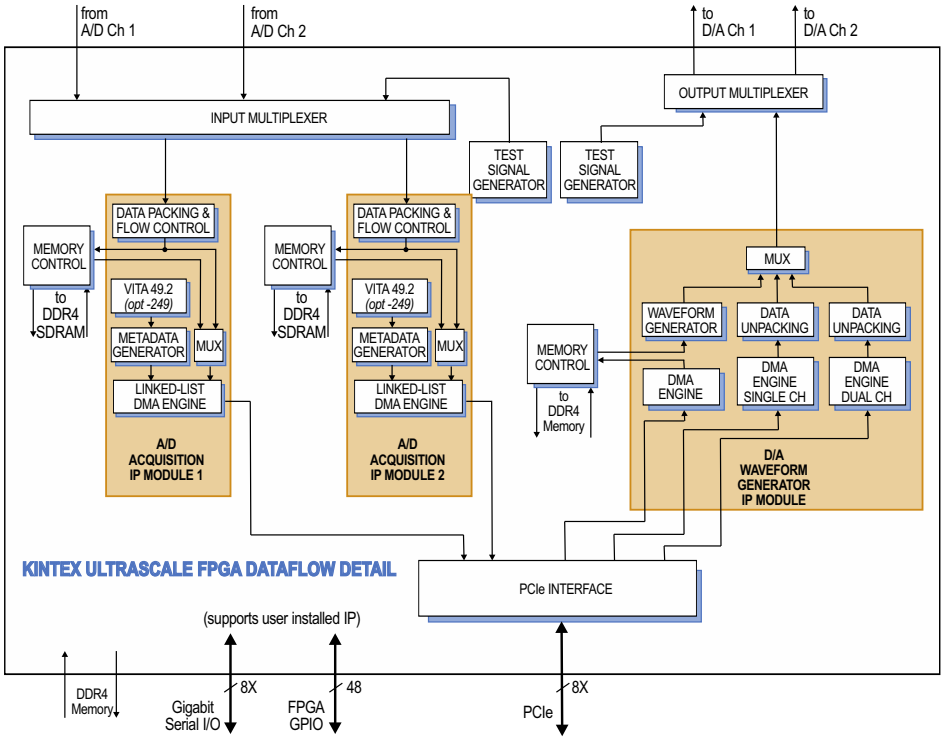
Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D's built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources. ➤



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Memory Resources

The 52141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 52141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek board-level products. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed. The system is equipped with sufficient power and cooling to ensure optimum performance.

Ordering Information

Model	Description
52141	1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
- 104	LVDS FPGA I/O
- 105	Gigabit serial FPGA I/O
- 249	VITA 49-2 support
- 702	Air cooled, Level L2
- 763	Conduction cooled, Level L3

Digital Upconverter and D/A

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Clocking and Synchronization

The 52141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5292 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -763: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 3U VPX board 3.037 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their many features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitiations.

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