

NAVIGATOR

Design Suite



MODELS 4814 & 4815 NAVIGATOR BOARD SUPPORT PACKAGE FOR LINUX & WINDOWS

- Includes C-language device libraries as well as high-level APIs
- Programming examples included to speed application development
- Full C-language source supplied with on-line documentation
- Complete control of hardware including all IP-based functions
- Signal Viewer for data display, validation, and monitoring

Navigator Design Suite

- Designed from the ground up to work with Pentek's [Jade®](#) and [Quartz®](#) architectures
- Supports Pentek's [ArchiTek™ FPGA Design Suite](#), which enables FPGA design engineers to add custom IP to a number of Pentek's [Talon® recording systems](#)
- Won a [Four-Star Best in Show Award](#) at the 2019 MTT International Microwave Symposium (IMS) Conference

MODEL 4811 NAVIGATOR FPGA DESIGN KIT

- Works together with Xilinx's [Vivado® Design Suite](#)
- Complete Vivado project containing all of the installed IP for the Jade or Quartz module
- Optimized for block design editing in Vivado
- 100% AXI4 compatible to simplify integration of custom IP and processing libraries from various sources
- All VHDL source supplied with on-line documentation and test benches

Overview

Pentek's Navigator® Design Suite includes the Navigator® FDK (FPGA Design Kit) for integrating custom FPGA logic designs or IP (Intellectual Property) into the Pentek factory-shipped design and the Navigator® BSP (Board Support Package) for creating host applications. The Navigator Design Suite takes a new approach to solving FPGA IP and control software connectivity.

Most modern FPGA-processing applications require development of specialized FPGA IP to run on the hardware, and software to control the FPGA hardware from a host computer. ➤

Even when “turnkey” solutions are delivered with complete FPGA IP and software libraries, as developers add their own custom-processing IP, new software needs to be created to control the custom IP functions.

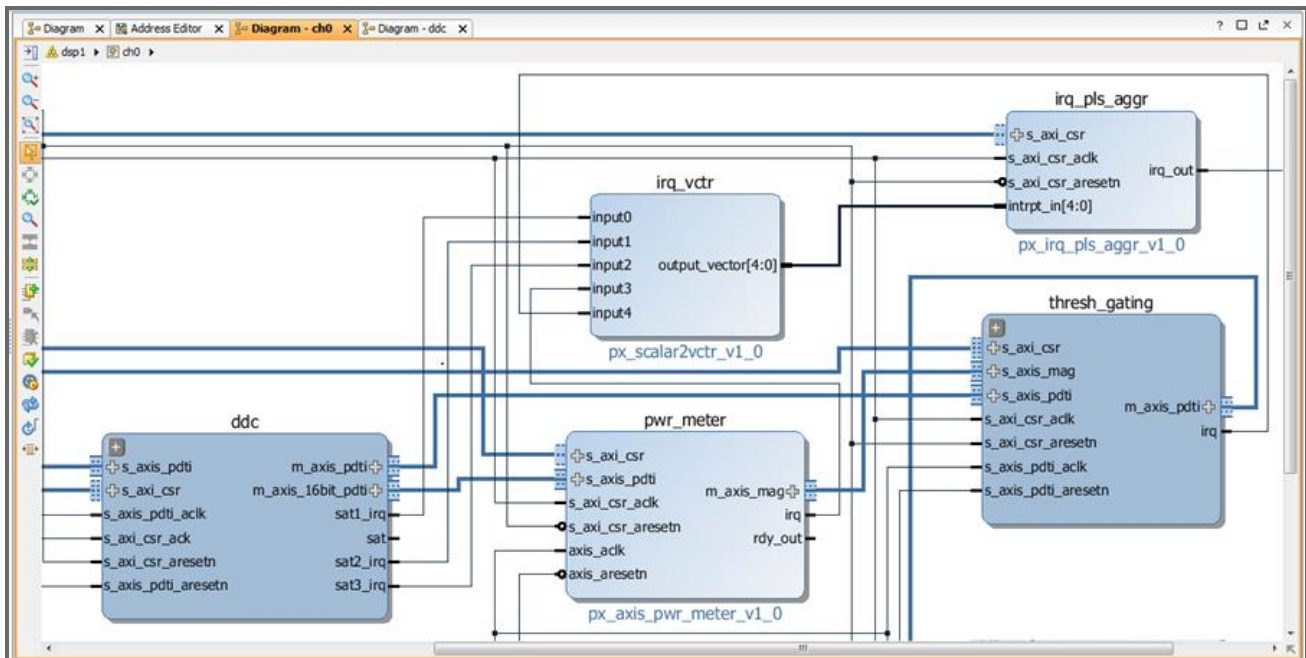
Problems often arise when the IP and software development tools treat application development as two separate tasks. Changes to FPGA IP and control software can quickly get out of sync, complicating new application development or even breaking the formally functioning turnkey components.

The Navigator Design Suite was designed from the ground up to work with Pentek’s [Jade](#) and [Quartz](#) architectures and provide a better solution to the complex task of IP and software creation.

Navigator FDK (FPGA Design Kit)

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater. The Xilinx Vivado Design Suite includes IP Integrator, the industry’s first plug-and-play IP integration design environment.

Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek’s Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

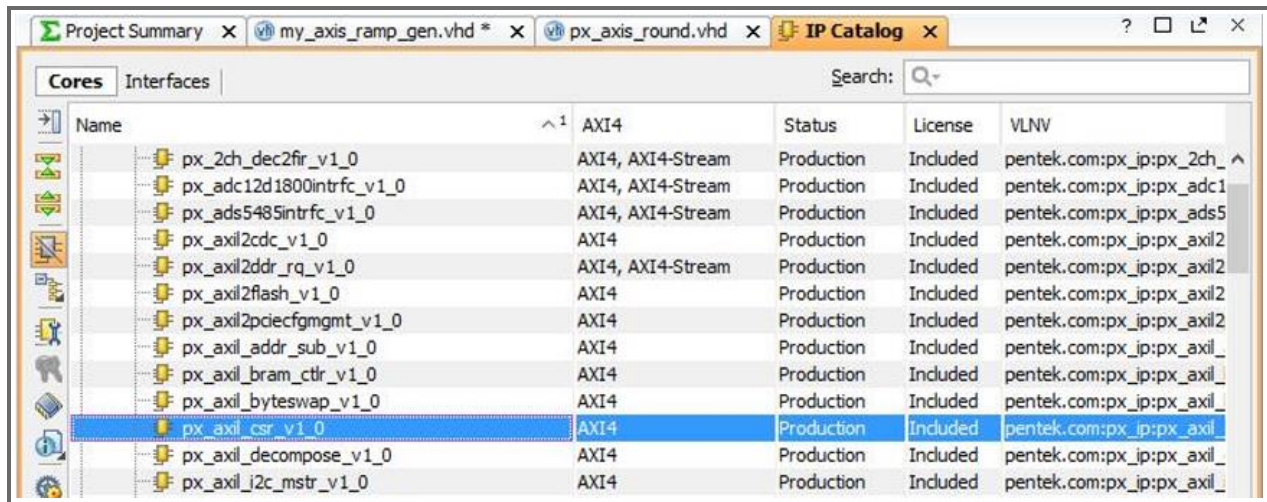


Pentek’s Navigator FDK opened in Vivado’s IP Integrator

All Pentek boards are shipped with a full compliment of built-in IP based functions for data acquisition, waveform generation and data tagging and streaming, and processing to match the hardware features of the board. Each Navigator FDK provides the complete IP design for the board it supports. When the design is opened in Vivado’s IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application. All blocks use industry standard AXI4 interfaces providing a well-defined format for custom IP to connect to the rest of the design.

The Navigator FDK includes complete documentation, test benches and full VHDL source for developers who desire complete access to the IP.

In addition to the IP specific to an individual supported board, the Navigator IP core library also includes IP blocks for many common general purpose functions. These include processing blocks for some of the most commonly used algorithms, data streaming blocks, data tagging and formatting blocks, and a 100 gigabit Ethernet UDP engine. All IP blocks are easily accessible within the IP Integrator interface from a pull-down list.



Navigator IP blocks are selectable from a pull-down list.

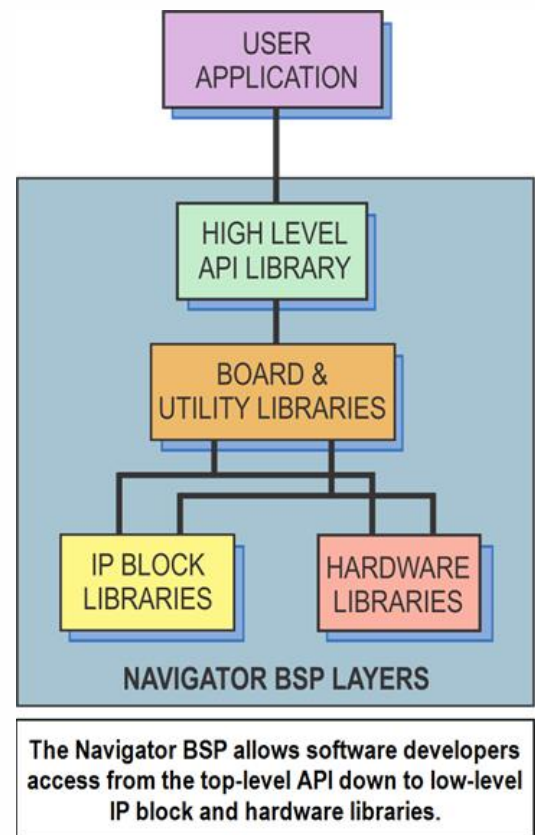
Navigator BSP (Board Support Package)

The companion product to the Navigator FDK is the Pentek Navigator Board Support Package (BSP). While Navigator FDK provides a streamlined path for creating or modifying new IP for the Pentek hardware, the Navigator BSP enables complete operational control of the hardware and all IP functions in the FPGA.

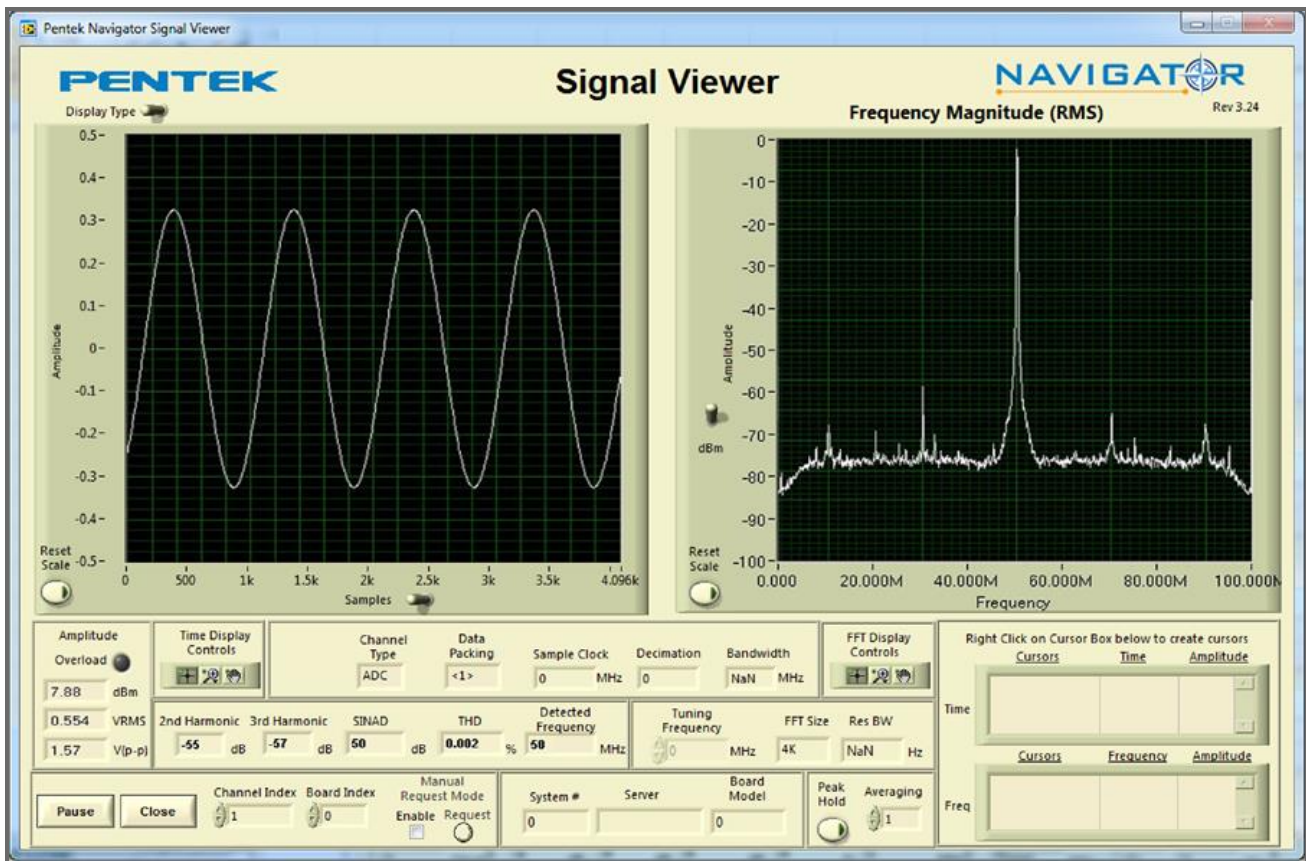
Similar to the FDK, the BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an intuitive API. The API allows developers to focus on the task of creating the application by letting the API and the hardware and IP-control libraries below it to handle many of the board-specific functions. Developers who want full access to the entire BSP library, enjoy complete C-language source code down to the lowest level as well as full documentation.

New applications can be developed on their own or by building on one of the included example programs. All Pentek boards are shipped with a full suite of build-in functions allowing operation without the need for any custom IP development. Many users find these functions ideal for addressing their application requirements.

The Navigator BSP includes the Signal Viewer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and



3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.



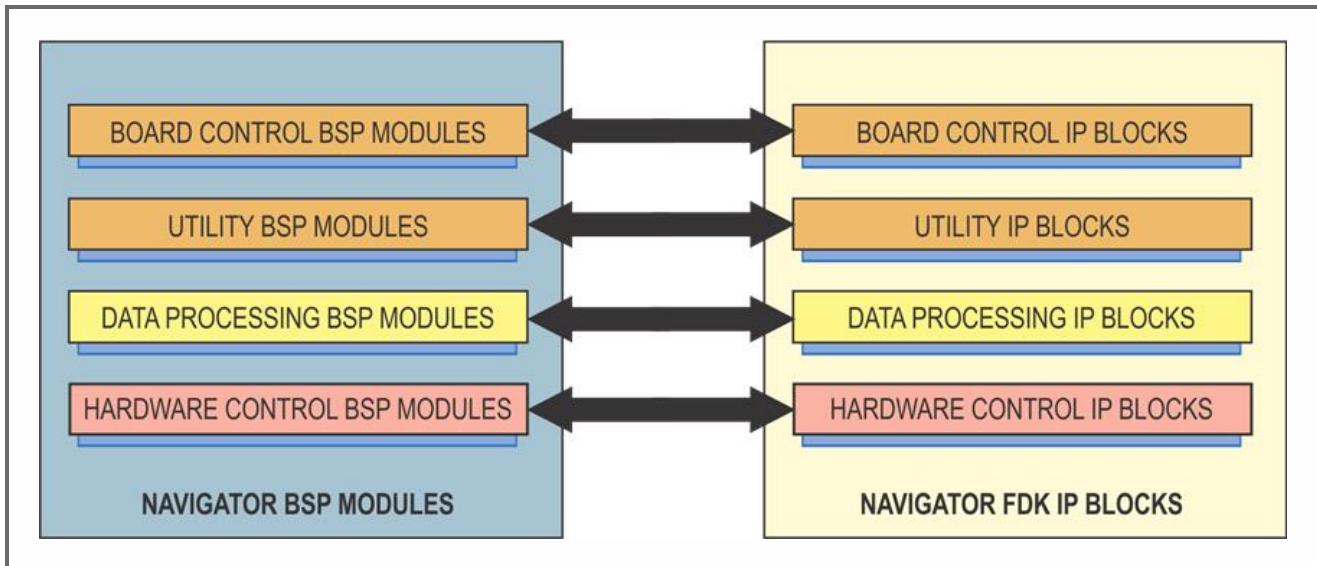
Navigator BSP Signal Viewer

Optimize BSP and IP Development

For users who need to develop applications that include custom IP, the combination and compatibility of Navigator FDK and Navigator BSP streamline development.

When new IP is introduced into the design, it has the potential of changing how the hardware looks to the host, possibly breaking the software. Navigator FDK and BSP were designed together to closely match the FPGA IP blocks and the BSP functions that control them. As developers modify IP they can easily find the corresponding BSP functions and modify them in parallel.

Navigator FDK uses AXI4 for all IP block interfaces. When developers create their own IP blocks using AXI4, they are immediately compatible with the Pentek-supplied IP. Following the Navigator BSP style guide, users can similarly create BSP modules for compatibility with the Navigator BSP library.

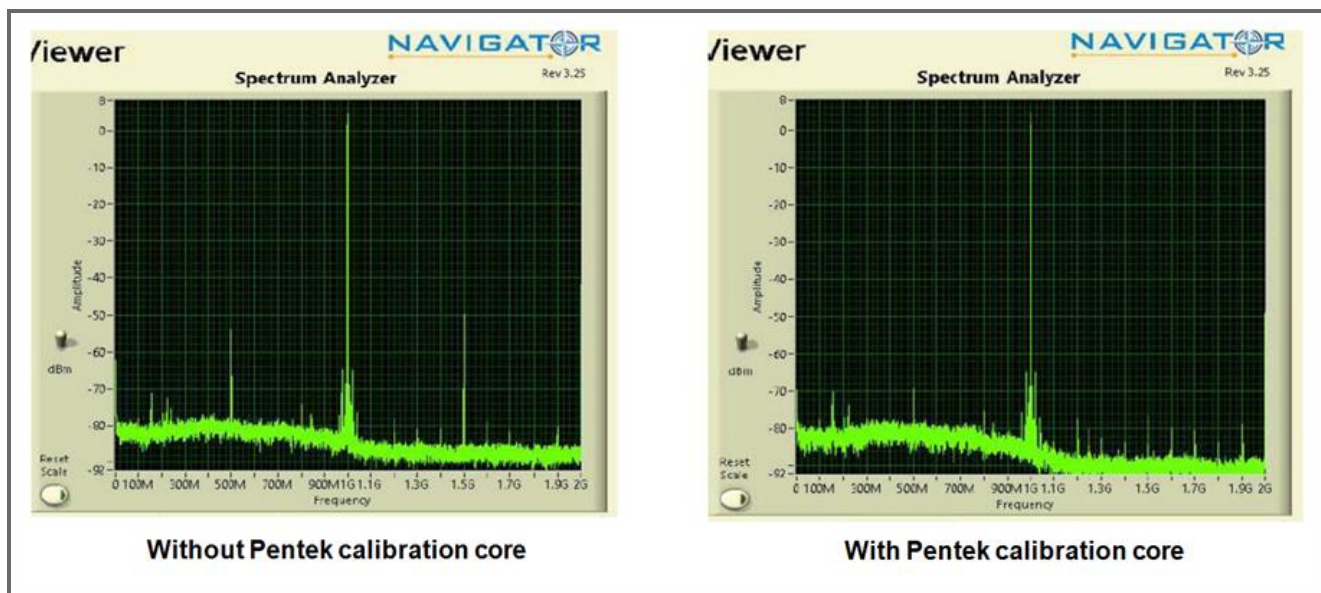


Optimized BSP and IP Development

Extended Support for the Quartz Family of RFSoc

Pentek's family of Quartz products based on Xilinx's RFSoc deliver an unprecedented amount of functionality in a single board. Both Navigator FDK and BSP have been extended to support this functionality.

Starting with the FDK, new cores have been added to fully support the RFSoc's on-chip A/D and D/A converters. Data acquisition and waveform generator cores have been updated and include support for VITA 49.2 packet formatting. A new optimized x16 decimation core has been added to supplement the RFSoc's built-in decimation. A Pentek designed A/D calibration core has been added to support on-board Quartz calibration hardware and improve the performance of the Xilinx recommended calibration core.



The test signal generator core supplied in previous version of the FDK, now includes a programmable sweep generator, ideal for quickly setting up radar test functions. All new cores for Quartz support operation of all eight A/D and D/A converters simultaneously.

In addition to data converter support, the Navigator core library now includes a 100 gigabit Ethernet UDP engine designed to provide a high speed path for moving data on and off the board through the Quartz board's optical interfaces. With each 100 GigE interface supporting sustained data rates of greater than 12 GBytes/sec, the board's dual interface provides greater than 24 GBytes/sec of data streaming.

The Navigator BSP has also been updated to include example programs for using the Quartz board's full set of hardware features and IP core functions. Each example can be used as is or can be modified for custom operation.

The Navigator BSP fully supports the RFSoc's ARM processors with Xilinx's PetaLinux. Software developers can run the Pentek examples or their own applications on the ARM processor under Linux. In addition to the example programs, the BSP includes a command processor application. With it running on the ARMs, the Quartz board can be controlled by commands received through the board's PCIe or 1 GigE interfaces. Pentek provides a full set of API commands for all the most commonly used functions. As with all of the BSP, the source code for this command processor application is provided allowing developers to expand the API set as needed to support custom functions.

ArchiTek FPGA Design Suite

The Navigator Design Suite supports Pentek's [ArchiTek™ FPGA Development Suite](#). ArchiTek allows FPGA design engineers to add custom IP to a number of Pentek's [Talon recording systems](#).

FPGA IP can be added to the recorder to provide real-time, on-the-fly digital signal processing during the data acquisition process, greatly reducing the time associated with post-processing recorded data. ArchiTek provides a simple development environment that allows engineers to add FPGA IP such as threshold detection, spectral filtering, digital downconversion, demodulation or any other digital signal processing technique required.

ArchiTek works together with Pentek's [Navigator FPGA Development Kit \(FDK\)](#) and [Board Support Package \(BSP\)](#) to provide a simple development environment that steps engineers through the process of integrating custom IP into the recorder. It includes [SystemFlow API](#) extensions and example projects that demonstrate custom FPGA IP integration along with modifications to the recording system's control interface.

ArchiTek also allows FPGA developers to add channels to the recording system, so users can record both processed and unprocessed data simultaneously. ArchiTek provides extensive documentation and tutorials to assist developers through the customization process, reducing risk along with development time.



Jade and Navigator

To view a video about how Navigator is used in conjunction with Jade products, click the image below.



Documentation for the Navigator Design Suite

User documentation for the Navigator BSP is provided as part of the user documentation for the Pentek Jade or Quartz board.

A Navigator FDK is created for each Pentek Jade or Quartz board and is available separately and includes the *Navigator FDK User's Guide* which describes how to install and use the FDK software. In addition, an IP Core Manual is provided for each IP core in the FDK. These can be accessed via the Vivado IP Integrator.

Several helpful tutorials also are available by contacting sales@pentek.com:

- *IP Core Conventions Guide and Example Labs* (part number 807.48111)
- *Designing with the PDTI Type AXI-Stream Bus* (part number 807.48112)
- *Designing with the Navigator DDR4 SDRAM Access Interface* (part number 807.48113)

Ordering Information

Model	Description
4811	Navigator FDK (FPGA Design Kit); Jade, Quartz
4814	Navigator BSP (Board Support Package) for Linux; Jade, Quartz
4815	Navigator BSP (Board Support Package) for Windows; Jade

Pricing and Availability

To learn more about our products or to discuss your specific application please contact [your local representative](#) or Pentek directly:

Pentek, Inc.
 One Park Way
 Upper Saddle River, NJ 07458 USA
 Tel: +1 (201) 818-5900
 Email: sales@pentek.com



As a Certified Member of [Xilinx's Alliance program](#), Pentek has passed a comprehensive 320-point review of its technical, business, quality, and support processes and has committed engineers who completed the same rigorous training used by Xilinx Field Application Engineers worldwide.

Pentek continues to demonstrate years of expertise with Xilinx devices and implementation techniques that consistently deliver high-quality products and services utilizing the Xilinx programmable platforms.

Free Lifetime Support

All Pentek hardware and software products include free lifetime support. Answers to software, IP or hardware questions are just a phone call or email away. Pentek's application support staff is comprised of senior level engineers with deep knowledge of the hardware and development tools.

Pentek's [YourPentek webpage](#) allows users to set preferences for notifications of new documentation as well as hardware, software and IP updates. Whenever Navigator FDK or BSP is updated, users receive an email informing them of the update with the option to download the version.