

The Pentek Pipeline

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- **Feature:** Drawing from more than 30 years of experience in the electronics industry, Rodger Hosking shares key insights for selecting real-time embedded system products. Rodger discusses various aspects of hardware and development, as well as the vendors producing these products.



“By following some key recommendations in making product and vendor choices, integrators can avoid risks and significantly reduce time in their development efforts.”

~ Rodger Hosking, Vice President, Pentek

- **Product Focus: Pentek Enhances Navigator Design Suite for the RFSoc Quartz Architecture**
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Top Tips for Selecting Real-Time Embedded System Products

by Rodger Hosking

Deployed systems for military and defense applications require a specialized class of electronic components from vendors that can support the special needs of embedded systems integrators. Of course, the hardware products must operate across a wide range of operating modes and environments to deliver performance levels meeting critical objectives for deployed warfighting equipment. But other factors may be even more important.

Because each project is unique, good system development tools are essential for systems integrators to deliver operational systems to their final customers as efficiently and effectively as possible. The vendors of these hardware and software products must help customers choose the most appropriate products, support them during development, and then offer life cycle management solutions for continued product availability.

By following some key recommendations in making product and vendor choices, integrators can avoid risks and significantly reduce time in their development efforts.

Hardware Tips: Open Standards

Increasingly, DoD procurement requirements now mandate compliance with emerging open system standards for embedded hardware components. These include SOSA, CMOSS, MORA, and several others. Among the many benefits to the government are interoperability among vendors, faster deliveries, and competitive pricing. Instead of replacing an entire system for a new technology upgrade, open standards allow replacement of compliant modules more quickly and at far less >



cost, thus extending the useful life cycle of deployed systems.

By following open standards, vendors also benefit by focusing design and development efforts on their areas of expertise, while other vendors produce complementary and compatible products to round out the supply chain. This fosters government confidence in relying upon these open standards for future long-term programs.

Thermal Management

As silicon device geometries continue to shrink, the power dissipation per transistor or element tends to drop, but this is often offset by increased clock rates. In addition, more elements can fit in a given size package, which drives power per device back up. Fine-pitch ball grid array packaging boosts component density of printed circuit boards, often causing significant heat per slot in today's embedded systems.

When designing a new embedded system, it is imperative that designers identify heat sources for each module as early as possible. Fortunately, the popular VPX specification defines numerous available solutions, including forced-air, air flow-through, conduction-cooling, and liquid cooling. Choosing the appropriate thermal

management solution at the beginning of a project can avoid costly redesign cycles and serious delays.

Synchronization

A growing number of phased-array antenna applications, including 5G wireless, airborne and SAR radars, electronic counter-measure systems, and directional communication links, all require multiple-element antennas to support beamforming for receive and transmit. Each antenna element signal requires precisely controlled, programmable phase shifts relative to all of the other elements.

Each signal often connects to a dedicated data converter where DSP circuitry can easily handle these precise phase shifts. However, the data converters must acquire and generate each sample at exactly the same sample clock edge. For large arrays, the high number of elements may require synchronous operation across multiple boards or chassis to handle all the channels.

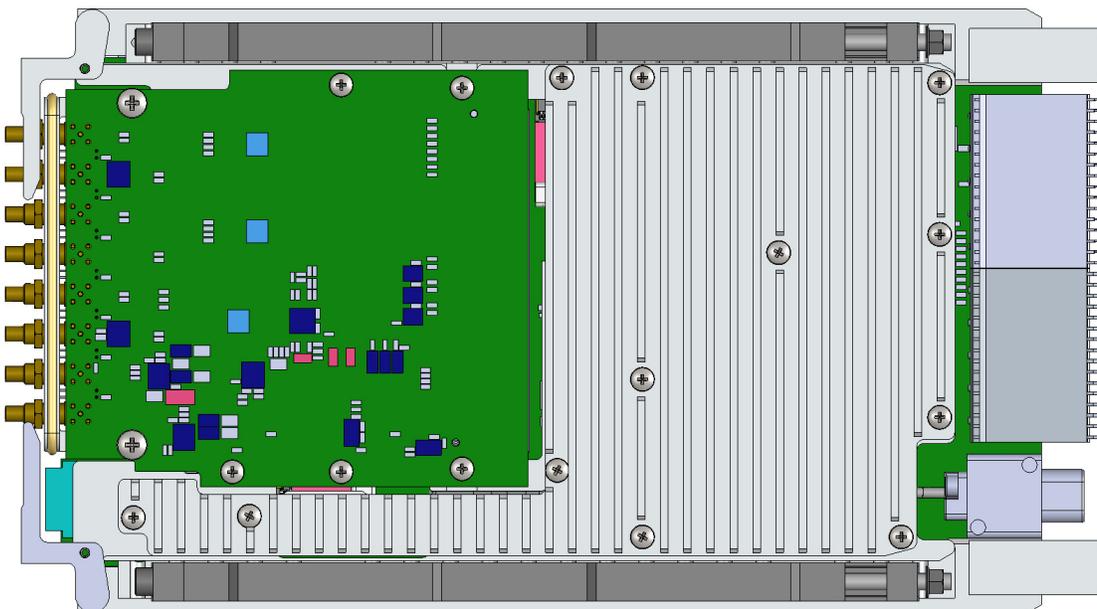


Airborne Radar

Such operation can only be achieved if this feature is part of the board design, and supported with timing and sync generators connected to each board. If channel synchronization is part of the system requirement, make sure the boards inherently include this feature with recommended connectors, cables, and sync generators, because synchronization is otherwise nearly impossible to add later.

Installed Features

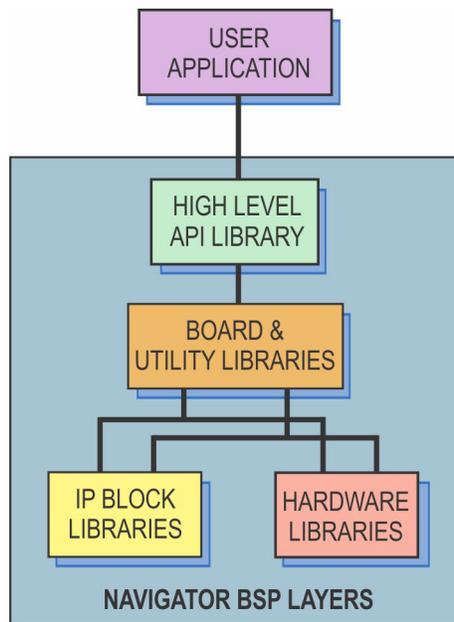
Real-time embedded boards playing typical roles in any system should include several basic functions supporting their assigned roles. For example, a single board computer (SBC) will almost always implement a PCIe root complex, system memory mapped across PCIe address space, network interfaces, and CPU peripheral I/O like USB, serial, and video. Standard CPU chip sets include virtually all of these functions, and supporting software drivers for Windows or Linux are commonly provided by the board vendor. ➤



Pentek's Conduction-Cooled Model 5983-313 VPX Board

Other boards, like FPGA software radio modules with A/D and D/A converters, have far different roles and requirements. Commonly needed functions here include triggering, gating, time-stamping, and synchronization engines that meet tight timing demands. Sample clock frequency synthesizers should accept a 10 MHz system reference from an on-board GPS receiver or external source. DMA controllers must move data between the data converters and system memory through a PCIe interface. Memory controllers for external SDRAM must buffer and capture real-time data converter streams, and communicate with the PCIe interface.

Unlike SBCs, which benefit from standard chip sets with low-level BIOS initialization, none of this exists for software radio boards. Instead, each of the hardware resources must be developed and incorporated in the FPGA. Equally important are the software libraries and drivers needed to make all of these resources work as required. Unless the board vendor includes them as factory-installed features along with the supporting software libraries, the system integrator must develop, design, test, and document this on his own. To minimize risks, expense, and uncertain delays, systems integrators should make sure the board vendor includes these important resources.



Development Tips: Software Development

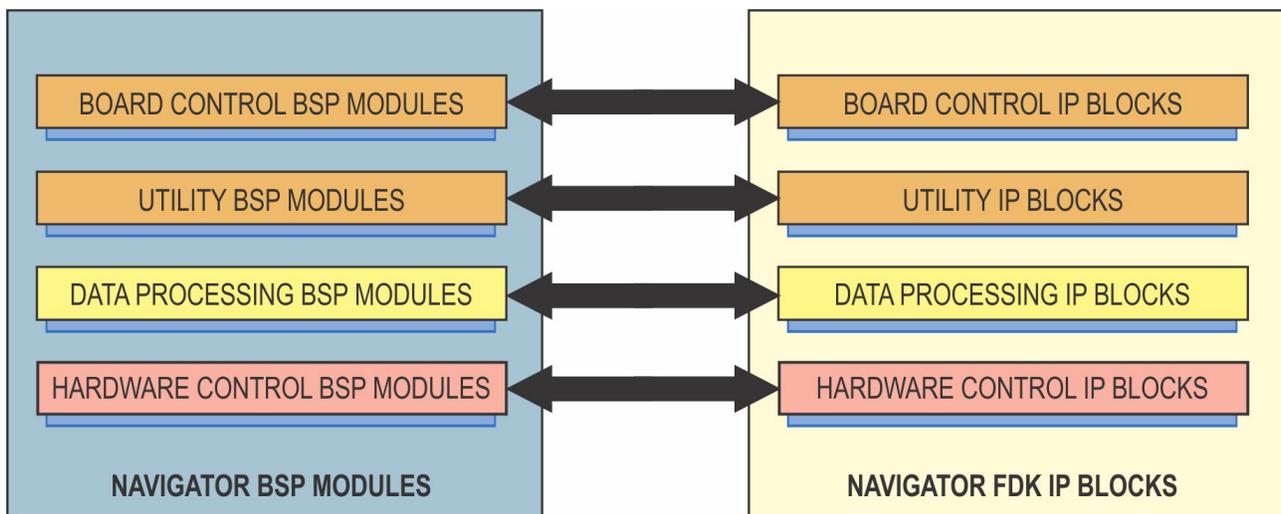
Although open system architectures help with electrical and mechanical interoperability, all real-time embedded systems are a collection of diverse hardware elements that must be carefully configured for a specific, unique application. Unlike mass market PC boards with plug-and-play capabilities, most embedded boards must be explicitly configured to perform specific tasks, told how to utilize specific external input, output and timing

signals, and instructed what, when, and how to communicate with other boards in the system. This is invariably accomplished by writing custom C programs that execute on the system controller, typically running the Linux or Windows OS.

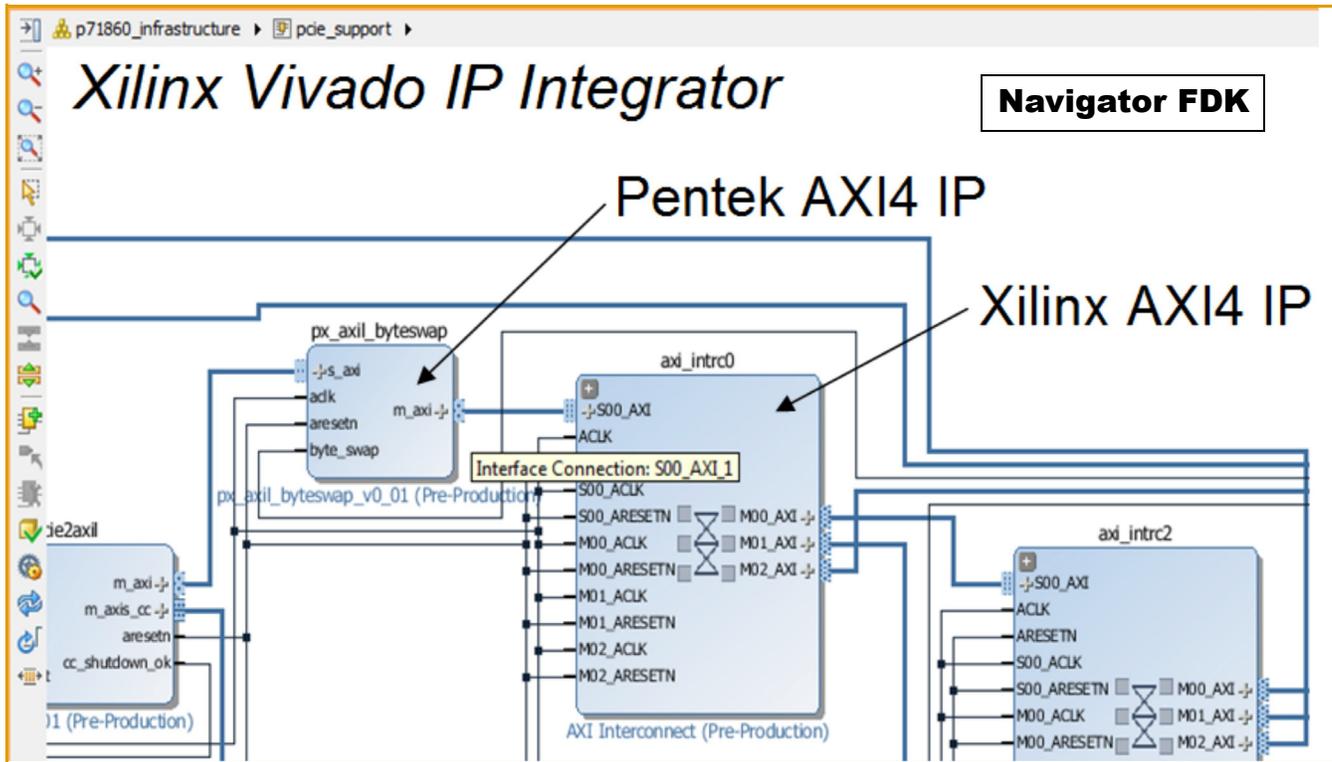
Even if an embedded board vendor provides C-callable functions for programmable hardware features, those offerings vary widely among vendors in their completeness and usability. Some offerings simply provide access to the programmable registers for the devices on the board, and the developer must use data sheets from the device manufacturer to figure out which bits to set. Even with a detailed block diagram of the board, this is very cumbersome.

In a far better approach, the board vendor offers high-level C libraries with well-documented command parameters that relate to the overall board-level operations performed, including references to other operations affected. Each of these high-level commands should include a well organized underlying collection of low-level libraries to allow modification for specialized operations.

An even more elegant offering is a true API (application programming interface) with an API command processor program running on the system controller. In this way, API commands can be sent to the controller where they are parsed and executed, without needing to recompile a ➤



Navigator BSP software modules and the Navigator FDK IP blocks they control are tightly linked to simplify custom IP development.



dedicated, executable C-program. API commands can be delivered to the controller via Ethernet, nicely supporting control and status functions of the embedded system from a remote client.

Lastly, numerous C program examples that illustrate typical operating scenarios are extremely valuable. They incorporate multiple high-level function calls with comments explaining the purpose of each, including why they must be executed in a specific order. Often these fully-tested examples can be incorporated directly into the final application to speed development. Of course, full C source code should accompany all library functions and code examples.

By selecting vendors offering these higher-level tools, systems integrators can complete their development tasks much more quickly and will be able to support changes and future upgrades far more easily.

FPGA Development

FPGA designs are really hardware designs, in which the basic hardware resources of the FPGA (thousands of gates, adders, multipliers, registers, switches,

memories, and interfaces) are wired together to create custom circuits. The wiring connection pattern is generated by software tools from the FPGA vendor that compile descriptive instructions from the designer to create a “bitstream.” When loaded into the FPGA, the bitstream implements the required interconnects for the required circuit, often simply called “IP” (intellectual property).

As mentioned earlier, the board vendor may install some standard IP functions at the factory. But many customers need to install additional custom IP within the FPGA for compute-intensive, real-time algorithms. These algorithms are often the systems integrators’ “secret sauce,” comprising their critical value-added contribution to the equipment. The ease of adding IP by the customer is highly dependent on the quality of the FPGA design package supplied by the board vendor.

First of all, look for a board vendor that includes most of the essential factory-installed features, like the ones described earlier. It will dramatically reduce the overall FPGA design effort. No one wants to spend years developing a JESD204 data

converter interface or a DDR4 SDRAM controller!

Next, be sure the board vendor supplies FPGA source code for all of the installed IP modules in the HDL format matching your FPGA designers’ capabilities: usually VHDL or Verilog.

Ideally, all IP from the board vendor will be delivered as AXI4-compliant blocks to match the style of reference IP blocks from the FPGA vendor. AXI4 is a widely adopted interface standard derived from ARM technology that tackles most of the housekeeping chores for connecting one IP block to another.

Take full advantage of the graphical design entry tools from the FPGA vendor, like Xilinx’s Vivado® IP Integrator. All of the AXI4 blocks are visually displayed, representing the entire block diagram of the project with all interconnects shown (see the illustration above). IP blocks and interconnects can be added, deleted, and modified with mouse clicks, and hyper-linked documentation is available by clicking on any block. After making the required changes, the project is recompiled to produce the new design and bitstream for the FPGA. ➤



Choose a board vendor that delivers the entire FPGA project folder containing all the files needed to create the delivered FPGA IP, fully AXI4 compliant, with complete documentation, and ready to compile using the FPGA vendor's tool suite.

Vendor Tips: New Technology

One of the major benefits of open standard COTS products is upgradability of existing systems with new technology by replacing a module instead of scrapping the system and starting over. Of course, depending on the upgrade, changes will often be needed to system software and perhaps even to some of the other hardware, interfaces, or connectors. Still, this is a well-proven strategy for extending the useful life of deployed equipment.

Choose board vendors with a history of consistently delivering open-standards products based on each new generation of FPGAs, data converters, memories, and system interfaces. Look for high-level development tools from those vendors to simplify the migration of software and FPGA designs.

Applications Support

Because every embedded system tends to be unique, systems integrators invariably encounter first-time configurations of multi-vendor products that don't seem to work as expected. Too often, each vendor blames another vendor for the problem, leaving the integrator on his own. Choose vendors with a proven track record of solving problems, regardless of who is at fault, and share such experiences with other project teams.

Most board vendors offer contracts to provide technical support during the development phase, although the quality and timeliness of that support varies

among vendors. When the support contract runs out, before they can get additional help, customers will either be asked to renew the contract, or for a credit card number. Some vendors offer free support for a limited time or number of hours, with payment required thereafter.

Be sure to ask any potential vendor for written descriptions of the applications support policies and costs before purchasing his products.

Life Cycle Management

One of the most significant problems for military program systems integrators is the increasing prevalence of component obsolescence, or end-of-life. This causes two major problems. Future component availability can jeopardize on-going production of enough boards to support multi-year installation program cycles. Also, 20-to-30-year maintenance contracts to support these fielded systems are at risk without the components needed for repairs.

Systems integrators naturally look to the board vendors for help, and various strategies have emerged. The simplest one is to purchase and produce enough additional boards up front to cover all installations over the life of the program, plus spares to cover the expected number of ➤



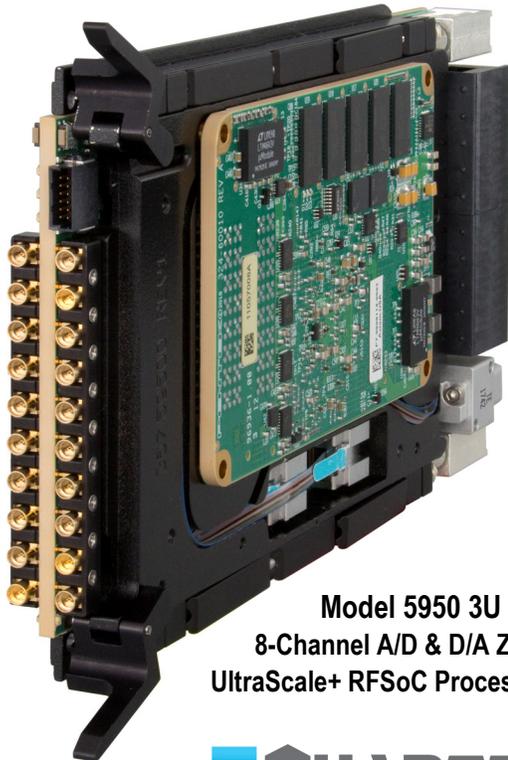
failures. End customers usually balk at the cost of this approach.

A very cost-effective alternative is a bonded inventory component program. The board vendor purchases all of the active components needed for production of the total number of boards required over the life of the program, plus extras for repairs. The vendor agrees to pay for these components, which the vendor reserves for him in bonded inventory. When production is required, those parts are used and their cost is credited towards the new purchase.

Since components like printed circuit boards and hardware can always be purchased as needed for later production, the cost of this bonded inventory program is a small fraction of the cost of full production up front, and very attractive to most customers.

Putting It All Together

As an example of these strategies developed over three decades, Pentek's latest offering is the **Model 5950 Quartz**



**Model 5950 3U VPX
8-Channel A/D & D/A Zynq
UltraScale+ RFSoc Processor**



Tech Talk: Development & Deployment Strategies for Xilinx's RFSoc FPGA

Development & Deployment Strategies for Xilinx's RFSoc FPGA

In this 30-minute webcast seminar, Rodger Hosking and Paul Mesibov, co-founders of Pentek, and Bob Sgandurra, Pentek's product manager, discuss how to unleash a powerful and unique RFSoc solution for addressing some of the most demanding requirements of high-bandwidth and high-channel-count systems.

[Click to view](#)

RFSoc 3U VPX module.

Following the VITA 65 OpenVPX standard, this powerful software radio board combines 8 channels of wideband A/D and D/A conversion, a wealth of Xilinx Zynq UltraScale+ FPGA resources, and a multi-core ARM processor to handle system controller functions.

Factory-installed features include IP for wideband data acquisition, triggering, timing, and multi-channel synchronization. A waveform generation engine creates analog signals from customer-created waveform tables or from an on-board frequency synthesizer and chirp generator. Linked-list DMA controllers move data from the board to and from the PCIe Gen. 3 x8 interfaces

and two 100 GigE interfaces, each capable of sustaining 12 GB/sec.

All of these resources are supported with software development tools under the Pentek **Navigator® Board Support Package**. It includes a high-level API, C-language libraries, a command processor for the ARM, complete C source code, and fully-functional starter applications.

For custom FPGA development, Pentek's **Navigator® FPGA Design Kit** contains the complete Xilinx Vivado project for the **Model 5950**, and a library of over 140 Pentek AXI4 IP modules for adding new features.

Pentek offers **free lifetime applications support** and well-developed **life cycle management** and **bonded inventory** programs.

By introducing a constant stream of industry-leading, open standard board level products with the latest data converters and FPGAs, Pentek helps systems integrators to take earliest advantage of the newest technology. □

Pentek Enhances Navigator Design Suite for the RFSoc Quartz Architecture

Pentek has introduced several enhancements to its **Navigator® Design Suite** for the **Xilinx® Zynq® UltraScale+™ RFSoc**. New IP expands Pentek's existing IP library to over 140 cores for FPGA development on its Quartz Architecture platform. Pentek's Navigator Design Suite includes the **Navigator® FDK (FPGA Design Kit)** for integrating custom IP into Pentek factory-shipped designs and the **Navigator® BSP (Board Support Package)** for creating host applications.

“The combination of the Navigator Design Suite and Quartz Architecture deliver some of the highest performance RFSoc FPGA designs available today,” said Robert Sgandurra, director of Product Management. *“These enhancements demonstrate our commitment to providing our customers with the best tools possible to optimize our hardware for their applications.”*

Extended Support for the Quartz Family of RFSoc

Pentek's family of Quartz products based on Xilinx's RFSoc deliver an unprecedented amount of functionality in a single board. Both the Navigator FDK and the BSP have been extended to support this functionality.

New & Updated IP Cores

Starting with the FDK, new cores support the RFSoc on-chip A/D and D/A converters with the following new features:

- Data acquisition and waveform generator cores have been updated that include support for VITA 49.2 VITA Radio Transport (VRT) packet formatting.
- A new optimized x16 decimation core extends the range of the built-in RFSoc decimation.



- Pentek's “smart” A/D calibration feature adds hardware, FPGA IP, and software to make Xilinx's calibration circuitry more robust across diverse operational scenarios.
- The programmable signal synthesizer core now includes a programmable frequency sweep generator, ideal for generating radar chirp pulse waveforms.

- These new cores for Quartz support operation of all eight RFSoc A/D and D/A converters simultaneously.

100 Gigabit Ethernet

In addition to data converter support, the Navigator core library now includes 100 gigabit Ethernet UDP engines, each moving data in both directions at 12 GBytes/sec through on-board optical interfaces. The Quartz board's optical interface supports up to two 100 gigabit Ethernet connections providing a total transfer rate of more than 24 GBytes/sec.

Updated Navigator BSP

The Navigator BSP adds new software resources for RFSoc ARM processors running Xilinx's PetaLinux. In addition to drivers, software modules and example programs, the BSP now includes an API command processor application so that Quartz boards can be controlled by high-level commands received through the board's PCIe or 1 GigE interfaces. Pentek provides a full library of API commands for all the most commonly used functions. As with all Pentek BSPs, full source ➤

2019 MTT International Microwave Symposium (IMS) Conference Awards

Pentek's Navigator Design Suite for Quartz was a 4-Star “Best in Show” Winner at the recent IMS Conference!



Military Embedded Systems contest winners are recognized for the improved performance and innovation they bring to military electronic systems applications such as radar and electronic warfare as well as for embedded computing and RF & microwave solutions. [Go to announcement.](#)

code for the API command processor application is provided so developers can expand or modify the API set as needed for custom functions.

The Navigator BSP includes new example programs for using the full set of evolving hardware features and IP core functions. Each example can be used as is, or its source code can be modified down to the lowest levels for custom operation.

Navigator Design Suite for Streamlined IP Development

Pentek's Navigator Design Suite was designed from the ground up to work with Pentek's Jade and Quartz architectures and Xilinx's Vivado Design Suite providing an unparalleled plug-and-play solution to the complex task of IP and control software creation and compatibility. Graphical

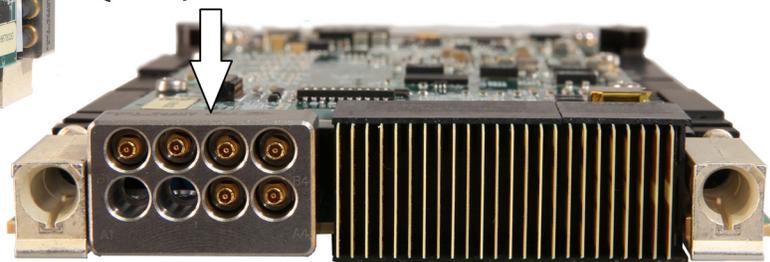
design entry for Xilinx and Pentek AXI4-compliant IP modules using the Xilinx IP Integrator greatly speeds development tasks. With a software library structure designed to match the structure of the IP cores, Navigator simplifies software development to support custom FPGA IP enhancements. The Navigator BSP is available for Windows and Linux operating systems. □



Model 54851: Pentek's New 3U VPX Board Optimizes High-Speed Optical and RF I/O Backplane Connectivity



← Option 111 - Rear Panel Connectors



Based on the Xilinx Kintex Ultrascale FPGA, Pentek's **Model 54851** features two 500 MHz 12-bit A/Ds with two programmable multiband digital downconverters (DDCs) and one digital upconverter (DUC) with two 800 MHz 16-bit D/As. The 54851 is the first board utilizing this new 3U VPX architecture with advanced wideband I/O options.

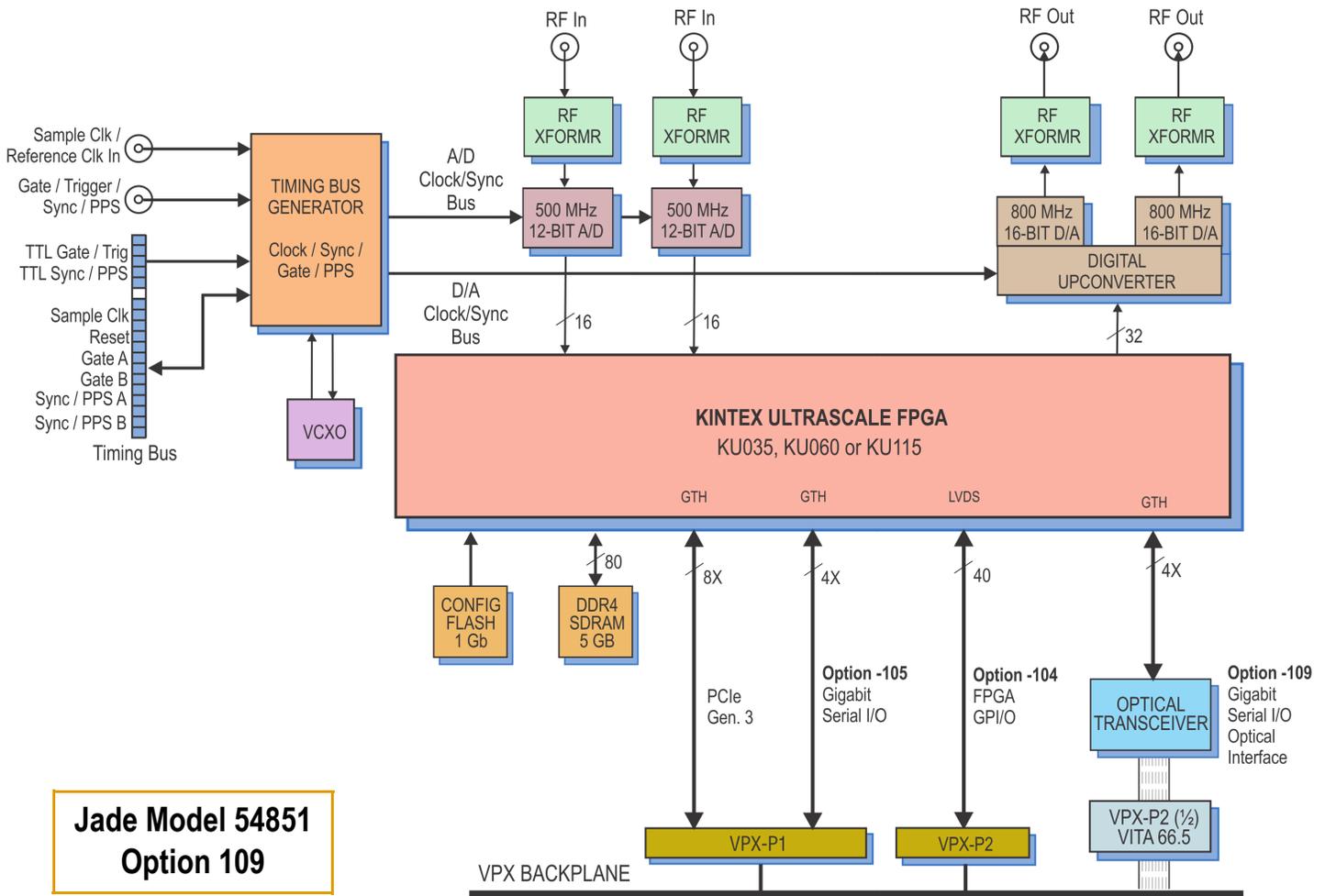
“Recent enhancements to OpenVPX have greatly improved I/O capabilities,” said Robert Sgandurra, director of Product Management. *“These enhancements play well into Pentek's modular approach to product design by offering optical and RF options for high-performance I/O that perfectly match our product capabilities.”*

Model 54851 takes advantage of these VPX I/O options for RF and optical interconnects through the VPX backplane:

- **Option -109:** Supports the emerging VITA 66.5 standard and provides four optical duplex lanes to a mating VITA 66.5 backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the VITA 66.5 interface enables high-bandwidth communications between boards or chassis independent of the PCIe interface.
- **Options -111 and -112:** Provide analog signal routing through the VPX backplane. Both options replace front panel connectors for RF In, RF Out,

Sample Clock/Reference Clock In, and Gate/Trigger/Sync/PPS In with coaxial signals which pass through the backplane for connections to other boards or chassis. Option 111 is compatible with VITA 67.2 and option 112 is compatible with VITA 67.3C.

Future options for higher density optical and RF connectors are planned as the supporting standards become available. Organizations such as The Open Group Sensor Open Systems Architecture (SOSA™) Consortium are proposing additional types and apertures for VITA 67.3C. ➤



**Jade Model 54851
Option 109**

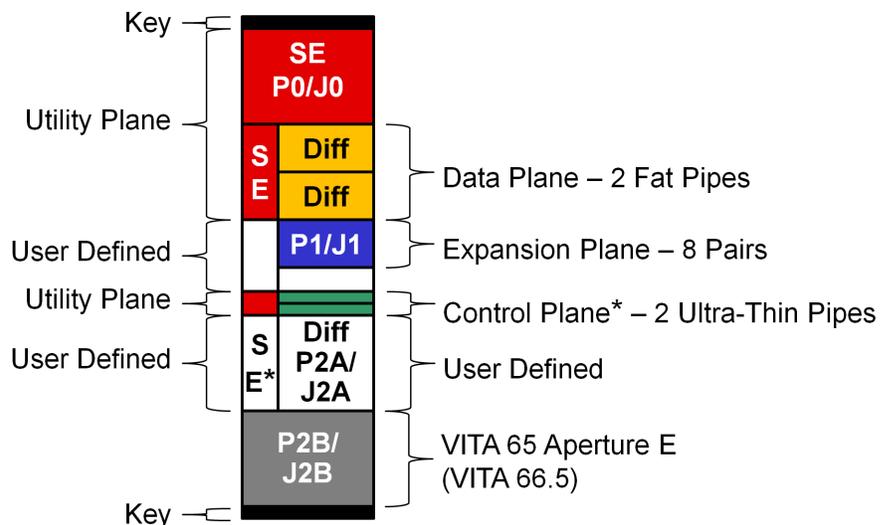
The Jade Architecture

Like all members of the Jade family, the 54851 is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 54851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

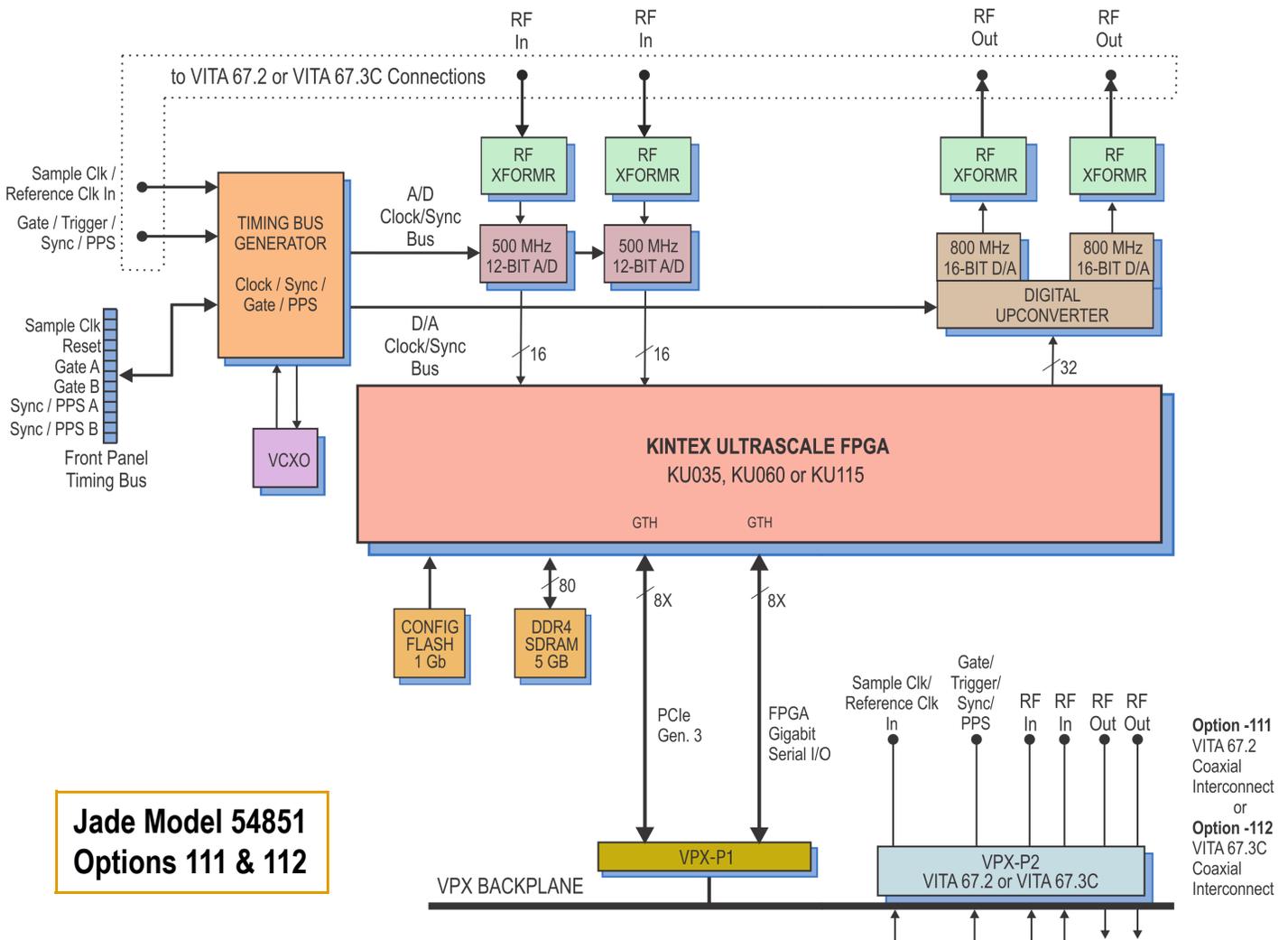
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited ➤

Slot Profile: Option 109 - SLT3-PAY-2F1F2U1E-14.6.6-1



* not connected on board



**Jade Model 54851
Options 111 & 112**

in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

For More Information

For more information about **Model 54851**, [click here](#). You also can email us at sales@pentek.com, contact **your local representative**, or contact Pentek directly [+1 (201) 818-5900]. □

Slot Profile: Options 111 & 112 - SLT3-PAY-2F1F2U1H-14.6.3-7

