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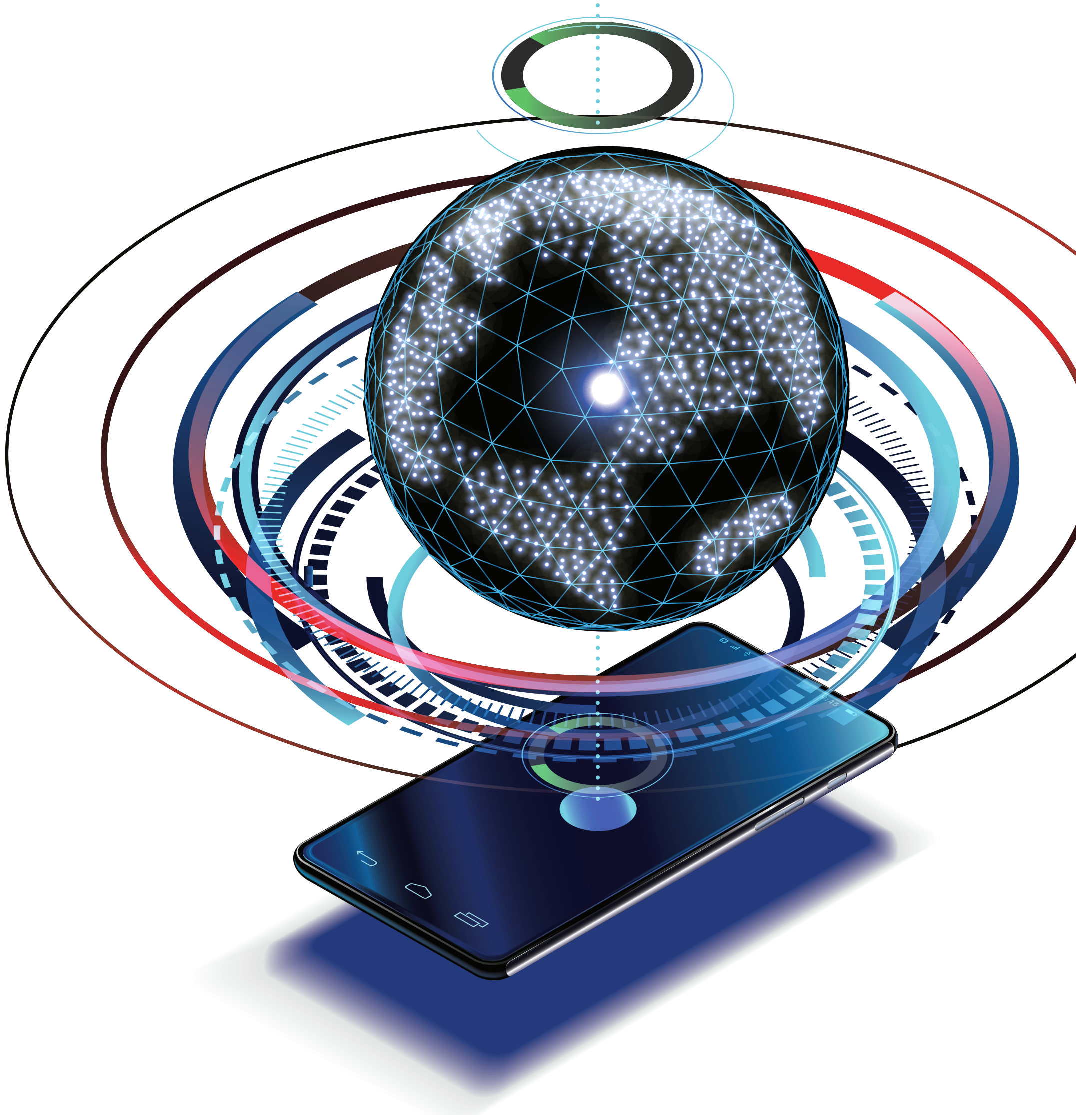

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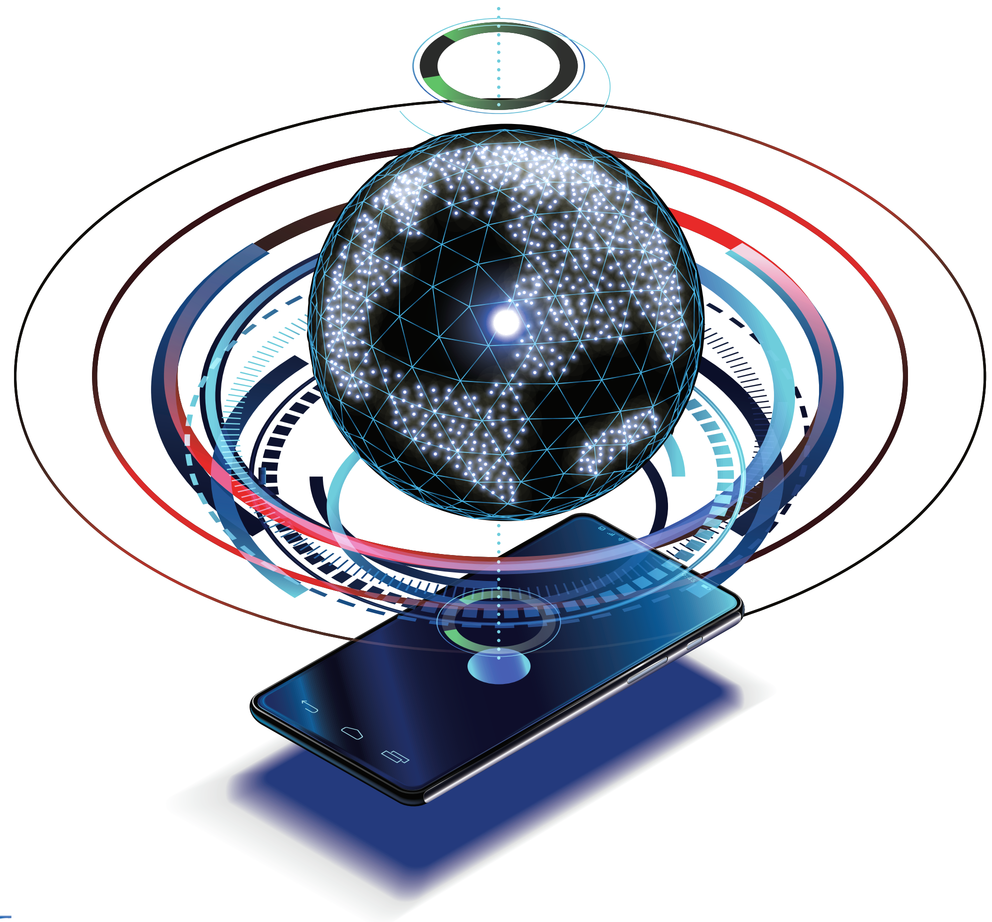
SDRs, ADCs, and DACs for High-Speed Communication



INSIDE

SDR's Hard Side Shown in DARPA Hackfest

By Tom Rondeau, *Program Manager, DARPA*

When I was running the GNU Radio Project before my current gig at the Defense Advanced Research Projects Agency (DARPA) began in 2016, I found it useful to bring the core developers from around the world together for a few days for what we referred to as our "hackfests." These gatherings gave us an opportunity to break away from our offices and day-to-day responsibilities to work out some of the larger technical problems that we were facing in the Project.

During these few-times-a-year hackfests, we worked crazy-long hours, lived on fast food, and de-prioritized sleep — an energizing combination that fostered collaboration and focused our attention in uniquely fruitful ways. As a result of some of our hackfests, core and prominent features were created that still reside inside GNU Radio today.

When I joined DARPA as a program manager, I found myself in a culture of audacious vision and hard work that enabled me to take the hackfest model to another level. The DARPA Bay Area Software-Defined Radio Hackfest, [held in November 2017](), focused on the idea of using commercial unmanned aerial vehicles (UAVs) outfitted with software-defined radio (SDR) to examine the future of programmable systems as well as the programmable electromagnetic spectrum.

In the weeklong hackfest, which we ran out of the NASA Ames facilities in Mountain View, California, we asked eight pre-qualified teams to take on different SDR/UAV missions to address problems that ranged from precise control of UAV movements to building UAV networks.

Out of the many decades of work on free and open-source software (FOSS) projects have come debugged and optimized software that is now helping us address technical challenges more quickly and effectively than we could before these tools became

available. Although this remains true, we learned from our hackfest experience in California that there still are many hard problems to solve.

During the hackfest, we saw teams struggle to master the combination of SDR and UAV technology against the background of real-world phenomena. Teams found that no matter how much FOSS is applied, they still had to confront a diversity of challenges, among them uncertainty and latency in moving the UAVs, computational limitations of embedded systems, different processor capabilities, and various issues with radio signals.

Teams experienced such challenges throughout the event. For example, the indoor environment by the range itself fluctuated as the doors opened and closed or as people moved around. That led to ugly radio frequency propagation issues from the concrete walls that surrounded the radios. Using an automatic system for power control or executing similar adaptive behaviors could have helped overcome the environmental changes.

When teams were initially developing their plans for taking on the hackfest missions, they often did not consider how real-world factors like indoor air currents would affect their designs. As such, they overlooked opportunities to apply well-known, though not often implemented, ideas to allow them to work better and faster.

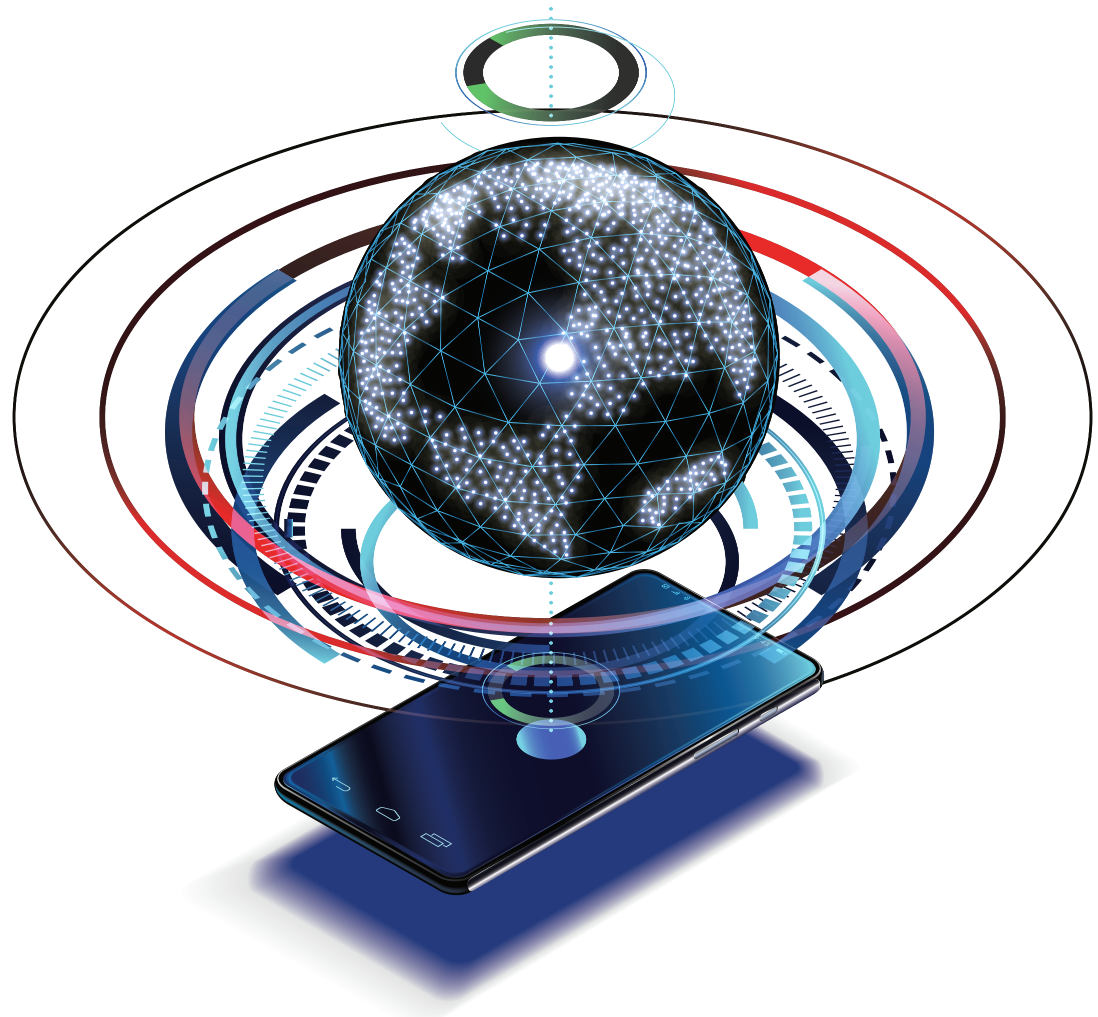
Software-defined radio has changed the conversation around how we engage the wireless world. To turn our ideas into reality, however, we must acknowledge the importance of practical physics, such as signal propagation issues like those in the Ames facility as well as the computational limitations of processing all of the algorithms relevant to ambitious goals such as marrying SDR and UAV technologies. Experience has proven that moving from a textbook or simulation into the real world is an exercise in which easy problems are hard to solve and hard problems are even harder to tackle.

The hackfest featured moderately hard challenges that, in reality, are very hard to meet successfully under time constraints. Despite working in a crucible-like environment riddled with unforeseen problems, the teams managed to rapidly innovate effective development practices and generate new knowledge about wireless systems.

FOSS and SDR have helped us come a long way in solving problems in the cyber-physical world, but as we learned from the hackfest, there is still much more to do. Based on my experience, hackfest-like contexts and the way that they concentrate innovative energy could be effective means for getting us there.

Direct-RF DACs for High-Speed Communications

By Bonnie Baker, *Applications Engineer, WEBENCH Design, Texas Instruments*



Consumers have an unquenchable demand for higher video, data, and voice bandwidths through the cable, satellite, and terrestrial conduits. For the next evolutionary step, consumers will want more bandwidth at a lower cost. To meet this challenge, OEM designers will need to offer communications equipment that supports higher capacity at a lower solution cost.

Modern wireless radio transmitter designs encompass real-intermediate-frequency (IF) transmitters, complex-IF transmitters, and zero-IF transmitters. At present, these transmitters continue to shuffle data through analog paths. There are limitations in the analog domain that impact the performance, capacity, and cost of the system, however.

To meet the demands for higher-bandwidth communications, IC manufacturers have developed direct-to-RF architectures that provide excellent spurious, low-noise performance with output update rates in the gigasamples-per-second (GS/s) range.

In this article, we will compare the direct-RF transmitter to the analog-RF structure. We will examine the evolution of the direct-RF, digital-to-analog converter (DAC) transmitter and see how it simplifies RF design and achieves higher capacity at a lower solution cost.

Analog complex-IF transmitter

Traditional transmitter architectures use the superheterodyne principle, wherein a local oscillator (LO) and a mixer generate IF. **Figure 1** provides a basic diagram of an analog complex-IF transmitter.

A complex baseband digital input signal commonly uses a low-voltage differential-signaling (LVDS) interface across two channels: an in-phase ("I") data channel, and a quadrature ("Q") data channel. Some systems use interpolation on the complex baseband I and Q signals by a factor R. Interpolation eases the requirements for the analog filter while also reducing in-band noise. The digital complex modulator and a numerically controlled oscillator (NCO) mix the signal in frequency ("heterodyning"). Dual DACs then convert the digital I and Q IF carriers into analog signals.

Now, in the analog domain, the two parallel signals flow through low-pass filters to their respective I and Q mixers. These mixers are fed by an LO, which has a straight-through I path and a 90° phase-shifted Q path. Finally, the two signals are combined through a summation block, resulting in a complex modulated signal at the desired frequency.

The use of this conventional transmitter architecture produces an LO "image" artifact. Before the final voltage-gain amplifier (VGA) stage, a bandpass or SAW filter is used to reduce the magnitude of the unwanted image. The filter rolloff must be

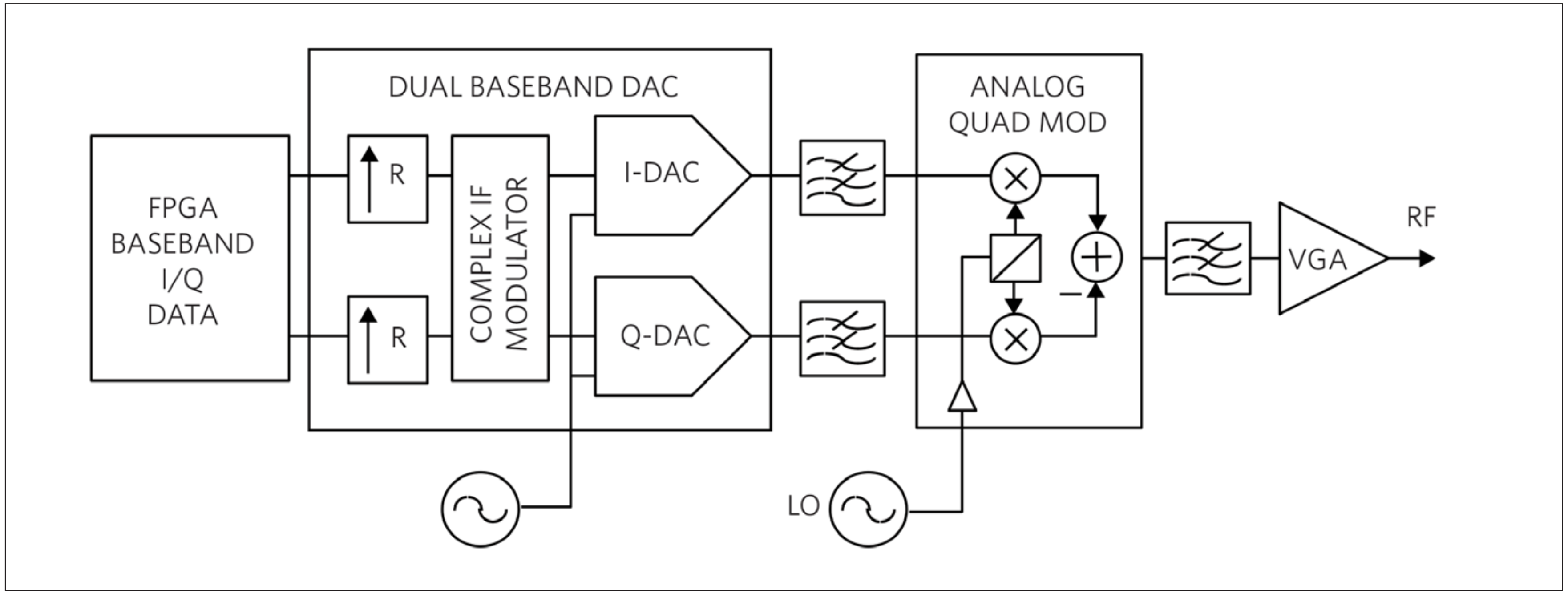


Figure 1: Analog complex-IF to RF-transmitter multi-device solution.

sharp and the LO frequency stable enough to reduce the unwanted sideband image (at fLO – fIF) without adversely affecting the desired signal (**Figure 2a**).

As **Figure 2a** shows, any analog mismatch (phase or gain error) between the I and Q paths results in a sideband image. In addition, the LO can feed through the mixing stage and appear in the RF output spectrum as LO leakage. These non-ideal artifacts limit the performance of an analog system, requiring additional filters and calibration circuitry, which, in turn, increases design complexity and cost.

This architecture has a limited output signal bandwidth because the input sample rate of the dual baseband interpolating DACs are constrained by the amount of data transferred over the relatively slow LVDS or CMOS interfaces. Often, this bandwidth limitation, in turn, requires different analog quadrature modulators (AQMs) or multiple sets of hardware, each with different LO frequencies, to support different RF bands.

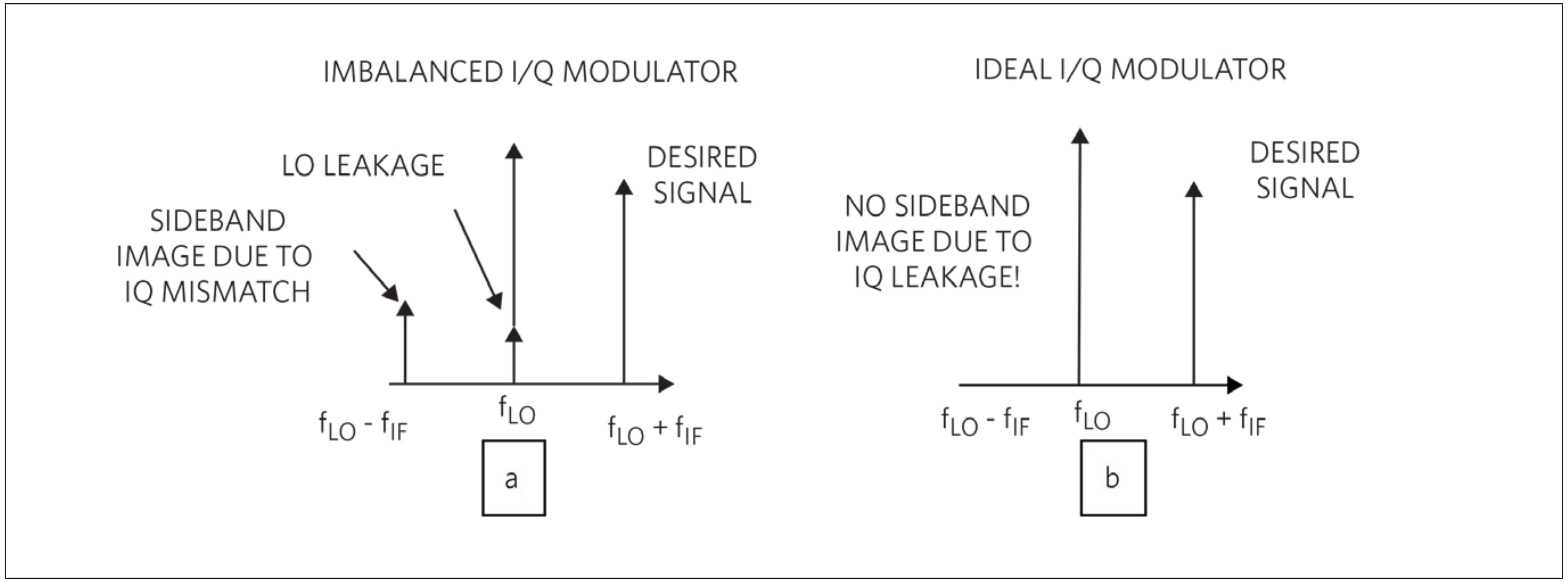


Figure 2: Non-ideal artifacts of an analog RF (I/Q) transmitter (a) versus an ideal direct-RF (RF DAC) transmitter (b).

Evolving to an RF-DAC solution

The baseband signal generated by the input is digitally up-converted using the I/Q interpolators, digital quadrature modulator (DQM), and NCO. The I/Q data paths in the DQM are perfectly matched (as a result of the digital implementation), which prevents the development of a sideband image (**Figure 2b**). The absence of the sideband image and LO carrier frequency eliminates the need for costly and complex SAW filters. The system then presents the signal to the RF-DAC core, which produces the RF output.

At the JESD204B input of the RF-DAC transmitter shown in **Figure 3**, the interpolators (↑R) increase the DAC sample rate relative to the input data sample rate.

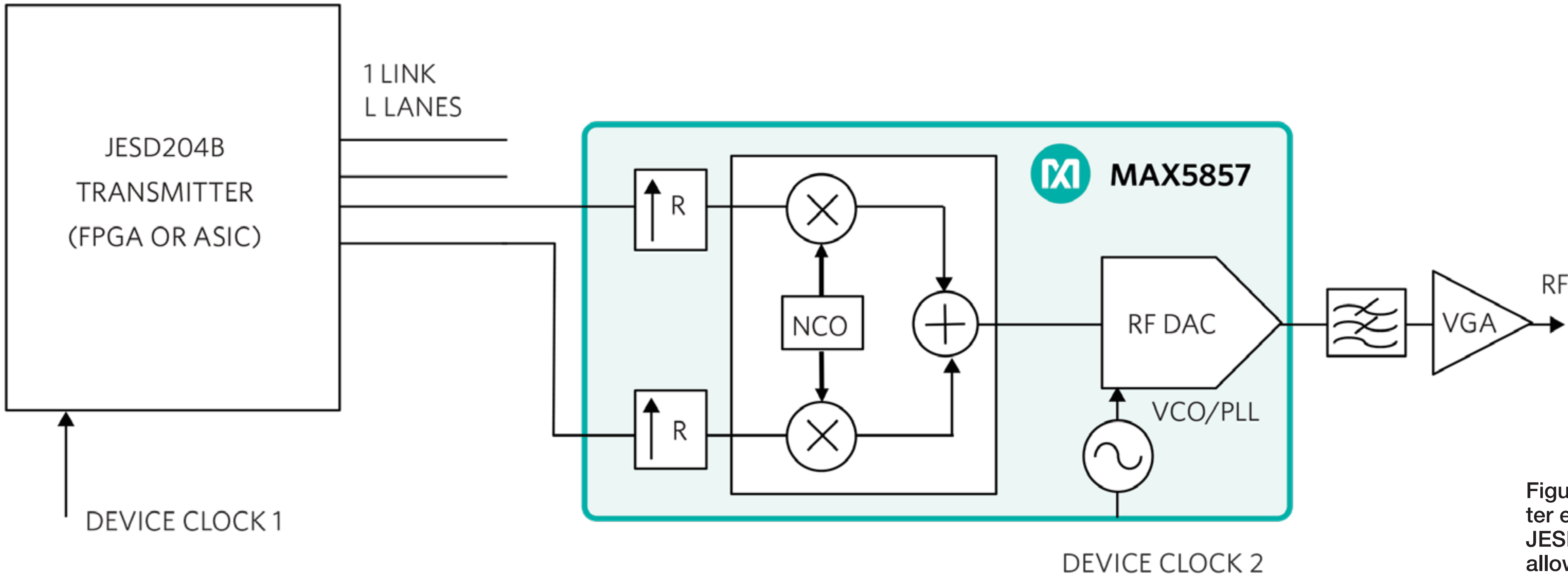


Figure 3: JESD204B input to RF-DAC transmitter enables higher input data sample rates. JESD204B is a high-speed serial interface that allows gigabits-per-second data rates.

The RF-DAC transmitter replaces the analog LO with a digital NCO, eliminating the LO feedthrough or leakage to the analog RF output. The output bandwidth of the RF DAC and the Nyquist bandwidth (fDAC/2) determine the maximum RF frequency.

The input structure of the RF-DAC transmitter accommodates high-speed 5G signals across the JESD204B serial interface, creating a system that has higher signal bandwidths than the analog complex-IF RF transmitter.

Compared to the analog complex-IF implementation, the RF-DAC transmitter architecture simplifies and reduces the cost of this application while increasing the bandwidth performance and reducing the PCB footprint.

Architecture comparison

The RF-DAC offers three opportunities to reduce the overall cost of the system, which includes PCB space, component count, and simplified design (**Table 1**).

The wave of the future in RF transmitters is before us. Although popular analog transmitter topologies are effective at lower frequencies with higher noise and cost, the speed of wireless data transmission is becoming beyond their capability. The next evolutionary step is the direct-to-RF transmitter. These interpolating and modulating 16-bit RF DACs provide improved spurious low-noise performance and simplified design. Their input data rates in the gigasamples-per-second region provides the high bandwidth requirements needed for 5G technology at a lower cost.

RF-DAC	Complex-IF
• Less Board Space	• Optimum Technology for Each Component
• Fewer Components	• Mature Technology
• Higher Production Yield	• Requires Unique Board for Each Band
• Simplified RF Design	• Calibration Circuit Needed to Reduce I/O image and LO Feedthrough
• No LO Feedthrough	
• No I/O Mismatch	
• GHz Bandwidth Feasible	
• Common Hardware for Multiple Bands	

Table 1: RF-DAC to complex-IF-transmitter comparison.

A Cryptographic Proof of Concept for Securing Aircraft ADS-B Data

By Sudhindra Nayak, *Senior Engineer, eInfochips,* **and Swaraj Chavan,** *Senior Engineer, eInfochips*

Automatic Dependent Surveillance-Broadcast (ADS-B) is a surveillance technology in which an aircraft uses a satellite navigation system to determine and periodically broadcast its position. The receivers then use these signals to track the aircraft in real time. ADS-B is an important part of the Federal Aviation Administration's (FAA's) next-generation (NextGEN) Air Traffic Control (ATC) system. By 2020, most of the aircraft flying into the United States needs to be equipped with ADS-B technology, according to the regulations set by the FAA. This push for equipping aircraft with ADS-B indicates the FAA's switch to a satellite-based navigation system from a traditional ground-based radio navigation system.

The current ADS-B system is implemented as an open protocol. Because the transmitted data is not encrypted in any manner, these can be read and decoded by an ADS-B receiver, including low-cost USB-based radio dongles like the RTL-SDR. With no security mechanisms in place to secure this data, this makes the system vulnerable to a variety of attacks. Hence, this whitepaper from eInfochips presents a cryptographic approach as a proof of concept to secure ADS-B data.

The system

With the ADS-B system, an aircraft uses a satellite navigation system to broadcast its position periodically. This information can be received by ATC ground stations to track the aircraft. This information can also be received by other aircraft in the vicinity, thereby providing situational awareness.

ADS-B data is transmitted every second. This makes the aircraft visible at all times to any ATCs and ADS-B–equipped aircraft in its vicinity. This data can further be used for post-flight analysis.

DF (5 bits)	CA (3 Bits)	ICAO address (24 bits)	Data (56 bits)	PI (24 bits)

Number of bits	Bit numbers	Abbreviation	Name
5	1 - 5	DF	Downlink Format = 17
3	6 - 8	CA	Capability (additional identifier)
24	9 - 32	ICAO	ICAO aircraft address
56	33 – 88 [33 - 37]	DATA [TC]	Data Type code
24	89 - 112	PI	Parity/Interrogator ID

Figure 1: ABS-B message structure. (Image: Mode-S.org)

ADS-B consists of two components:

- ADS-B Out: This broadcasts data that includes aircraft identification, current position, altitude, and velocity through a transmitter onboard the aircraft.
- ADS-B In: This is the reception of ADS-B data from nearby aircraft for improved situational awareness.

An ADS-B system depends on a satellite navigation source for position determination and a data link. The data link operates at one of two frequencies: either 1,090 MHz or 978 MHz. Aircraft that operates below 18,000 feet (5,500 m) uses the 978-MHz data link, while commercial aircraft uses the 1,090-MHz link.

An ADS-B message is 112 bits long and consists of five parts, as indicated in **Figure 1**.

Security in ADS-B

ADS-B was developed to extend existing radar surveillance systems and eventually reduce dependency on those systems. Compared to traditional radar surveillance systems, ADS-B has better coverage over long distances like oceans because it sources its data from satellite navigation systems.

Security has been a concern in ADS-B ever since its inception. The FAA did a Security Certification and Accreditation Procedures (SCAP) study to address the security vulnerabilities in ADS-B. Based on this, the FAA stated: "Using ADS-B data does not subject an aircraft to an increased risk compared to the risk that is experienced today."

Because there is no security mechanism in place to secure this data, the system is vulnerable to a variety of attacks. Three possible attack scenarios are as follows:

Eavesdropping: The current ADS-B system is implemented as an open protocol.

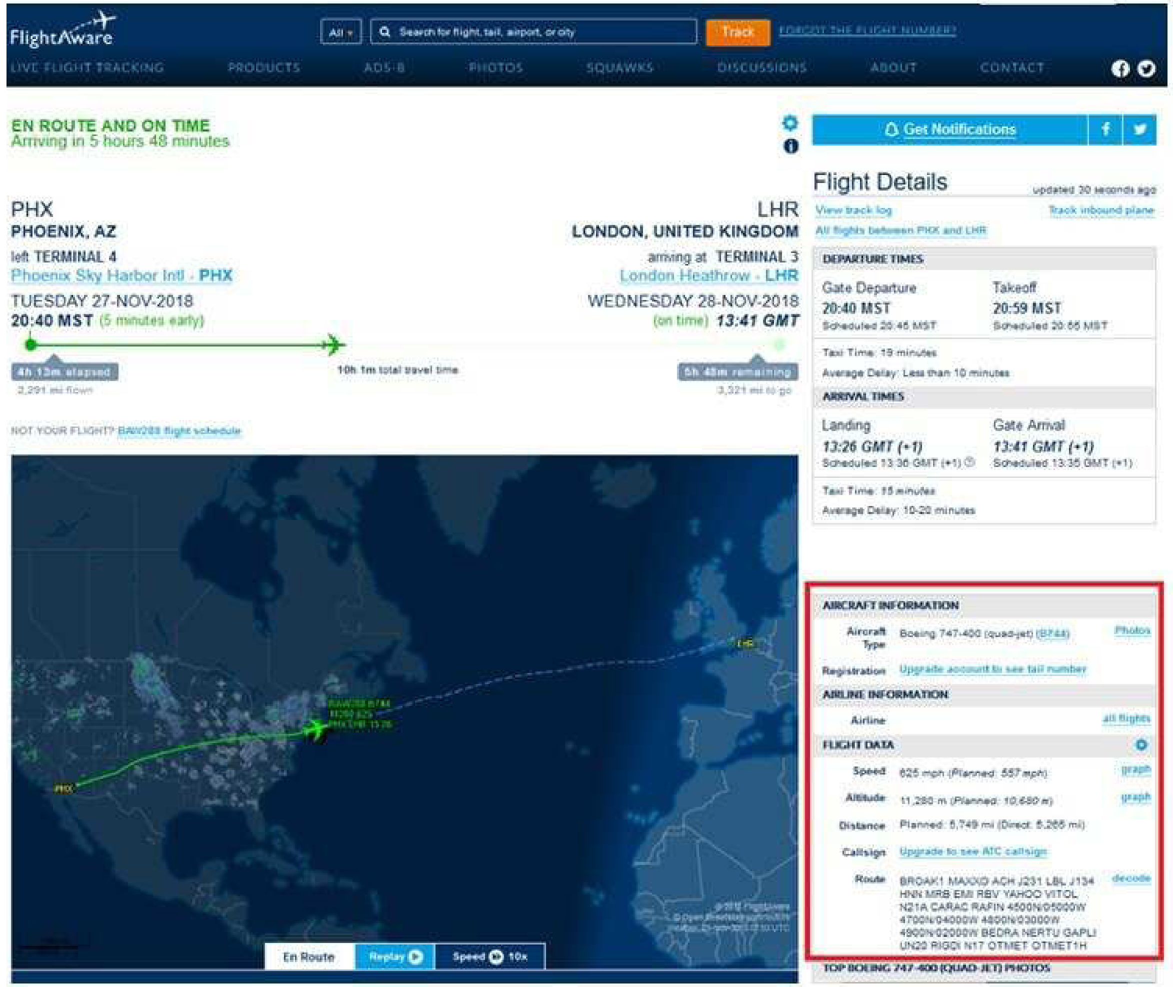


Figure 2 (Image: Screenshot of the FlightAware website)

Because the transmitted data is not encrypted in any manner, it can be read and decoded by any ADS-B receiver, including low-cost USB-based radio dongles like the RTL-SDR. Websites like FlightAware use crowd-sourced data to track aircraft in real time. A screenshot of the website is shown in **Figure 2**.

Jamming: The transmission of high-power signals in either of the 978-MHz or 1,090-MHz ADS-B data link bands can disable communication over the link.

Spoofing: The transmission of signals in either of the 978-MHz or 1,090-MHz ADS-B data link bands may use the ADS-B protocol to insert incorrect information. This would show up as a false aircraft.

The FAA mandating the use of ADS-B in an aircraft indicates the intention to move from traditional radio-based navigation aids to satellite-based navigation aids. With the FAA's mandate to equip most aircraft flying into the U.S. airspace with ADS-B by 2020, the need to address these security concerns is now even greater.

To mitigate these security risks, a cryptographic approach that could be used to secure ADS-B data has been developed. This has been demonstrated through a proof of concept, as discussed in the following sections.

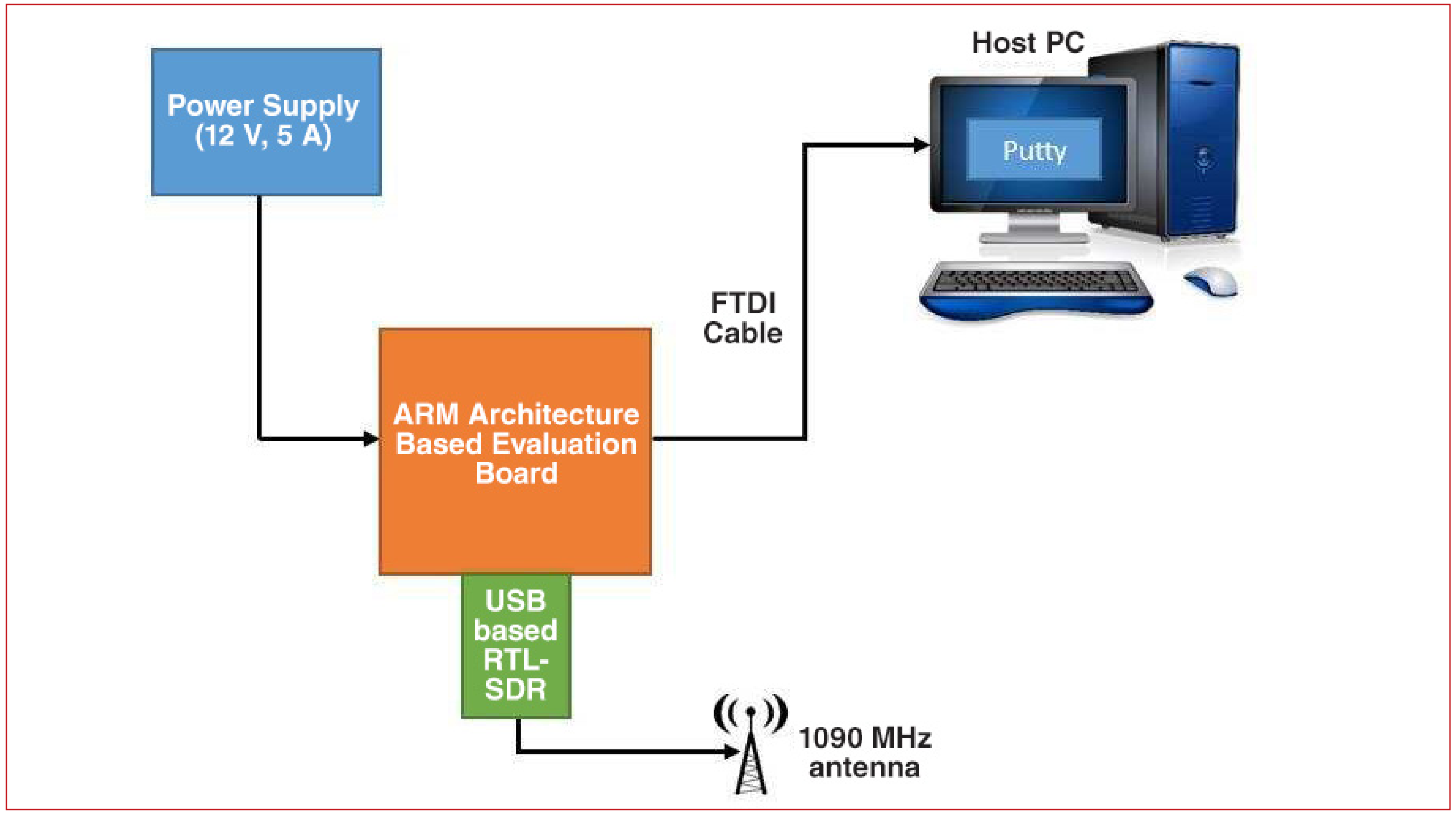


Figure 3: Block diagram of evaluation setup. (Image: eInfochips)

A proof of concept to secure ADS-B data

To demonstrate the concept of securing ADS-B data with a cryptographic approach, a low-cost software-defined radio (SDR) — like the RTL-SDR — was used along with a 1,090-MHz ADS-B antenna. The antenna received ADS-B signals from the aircraft in its vicinity, and these signals were processed in the SDR. The SDR was connected to an Arm architecture-based evaluation board. The encryption and decryption algorithms were run on the evaluation board. The setup used is illustrated in **Figure 3**.

Algorithm implementation

To start off, an open-source software project, rtl-sdr, was used to get a data dump (IQ samples) of the encoded ADS-B data transmitted by the aircraft. A proprietary symmetric-key encryption algorithm was developed and implemented in Python to encrypt and decrypt this data. The decrypted data was then decoded using an open-source ADS-B signal decoder called dump1090 to check the validity of the output data. This was a file-based implementation in which the encryption and decryption were performed on ADS-B data-dump files.

The implementation illustrated was realized on an x86 architecture. Considering the widespread use of Arm-based architectures in avionic navigation systems, it was decided to test this proof of concept on an Arm architecture-based system. Taking into consideration the extensive use of C++ in the avionics system software, C++ was considered for this implementation. Hence, the original algorithm was later re-implemented in C++.

The open-source ADS-B signal decoder dump1090 source code was modified to decode a live ADS-B data stream. The implementation of the encryption and the decryption algorithms were developed as libraries that could be linked and used.

Algorithm performance

To measure the algorithm's performance, the time taken to encrypt and decrypt the data dump of a known size was determined. Optimizations were applied to the implementations to reduce the time taken to encrypt and decrypt the data. A summary of the algorithm's performance after optimization for different file sizes is summarized in **Table 1**.

File size of data dump	Number of ADS-B packets	Encryption time (milliseconds)	Deccryption time (milliseconds)
713 KB	194	150	170
1.3 MB	3 (due to less air traffic)	270	310
3.7 MB	10 (due to less air traffic)	650	740

Table 1: Summary of the algorithm's performance. (Image: eInfochips)

Simulink-based implementation

The above proof of concept was also implemented as a model-based design in Simulink. The ADS-B example in Matlab was used as a starting point for this implementation. The proprietary algorithm was implemented as Simulink blocks. This model was run on an x86 architecture and also on a Raspberry Pi using the hardware support packages for Raspberry Pi in Simulink.

Use case

Original equipment manufacturers (OEMs)

that develop software for ADS-B transponders can add the encryption algorithm to their software, thus enabling the ADS-B data being transmitted to be encrypted. This data can be decrypted by only those receivers that have the secret cryptographic key to decrypt this data.

This feature can be made optional by enabling or disabling it based on the aircraft's requirement. To make this feature optional, the implementation of the encryption algorithm in the transponder source code can be conditionally compiled to enable or disable this feature. Aircraft manufacturers that install the OEM's products can provide the airlines buying their aircraft with an option to enable/disable this feature, thereby allowing the airlines to decide whether or not to encrypt their aircraft's data.

Disclaimer

The encryption and decryption of ADS-B data described in this article is not a solution that has been approved by regulatory authorities like the FAA. Through this proof of concept, we are offering a solution to secure these communications, but the standard ADS-B protocol is not modified in any manner. We are adding an additional security layer without compromising the processing efficiency of the ADS-B data.

Conclusion

ADS-B is a system with many security risks, making it vulnerable to a variety of attacks. However, due to the FAA's mandate to upgrade or install ADS-B hardware in aircraft, it is important to address these security concerns. The cryptographic approach discussed in this article can provide a good solution to overcome concerns related to the security and sensitivity of this airline data.

Resources

White Paper: Strategies for Deploying Xilinx's Zynq UltraScale+ RFSoC

Podcast: RFSoC Enabling Radar/ Electronic Warfare Systems

Technical Handbook: Critical Techniques for High-Speed A/D Converters in Real-Time Systems, 12th Edition

Technical Handbook: Software-Defined Radio Handbook, 14th Edition

Technical Handbook: High-Speed Switched Serial Fabrics Improve System Design, 10th Edition

Technical handbook: Putting FPGAs to Work for Software Radio Handbook, 12th Edition

White Paper: Development Tactics and Techniques for Small Form Factor RF Signal Recorders

Signal Chain Basics: RF-Sampling ADCs for Multiband Receivers

By Robert Keller, *Systems Manager, Wireless Infrastructure Group, Texas Instruments*

High-speed data converters can now digitize or generate signals directly at radio frequencies (RFs), replacing traditional RF components such as mixers and local oscillators (LOs) with digital processing. In addition, the wide-bandwidth capabilities of RF-sampling data converters with multiple gigasample-per-second (GS/s) speeds enable radios to combine multiple bands for cellular infrastructure applications, resulting in smaller and lower-power systems that can ultimately reduce the number of remote radio head (RRH) boxes at each cell site. My previous article, "Signal Chain Basics #131: RF-sampling DACs for multiband transmitters" focused on RF-sampling transmitters; this article will cover ADCs and receivers.

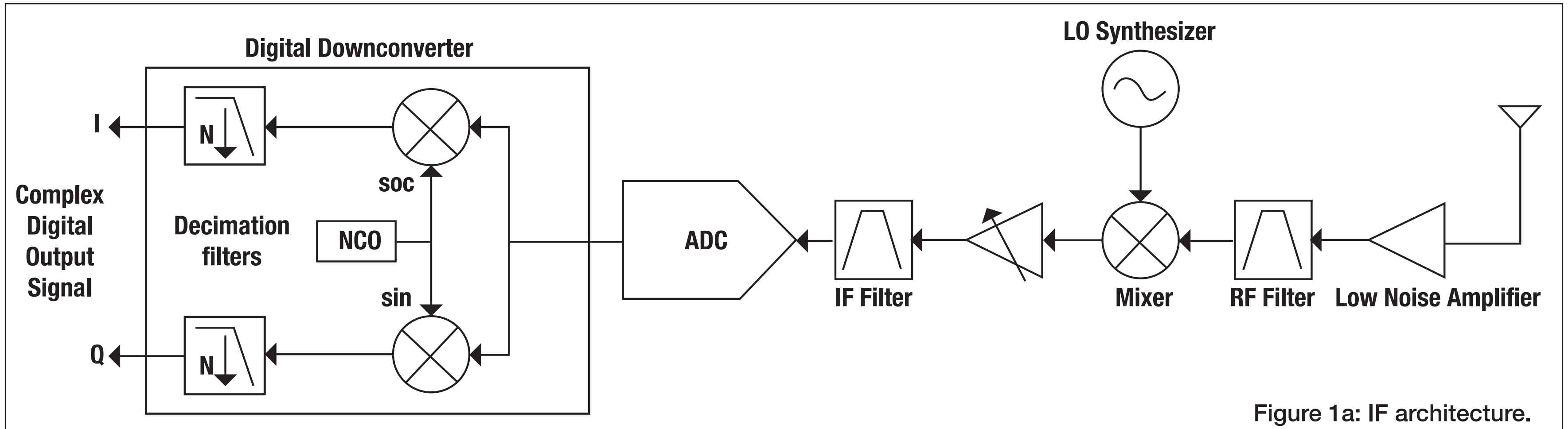


Figure 1a: IF architecture.

Traditional radio architectures use either an intermediate frequency (IF) architecture (**Figure 1a**) or a zero-IF architecture (**Figure 1b**). In an IF architecture, the signal from the antenna is amplified and down-converted with a mixer to an IF, typically about 10% of the RF. A variable gain amplifier amplifies the IF signal, which passes through a band-pass filter before being digitized in the analog-to-digital converter (ADC). IF architectures are usually built from discrete components because it is difficult to integrate an IF filter.

In a zero-IF architecture, an analog quadrature demodulator amplifies and down-converts the RF signal directly to baseband. After filtering, a dual ADC converts the complex analog signal to a digital signal. Given the baseband ADC and low-pass baseband filters, a zero-IF receiver lends itself to integration.

Figure 1c illustrates an RF-sampling architecture. The end-to-end functionality is the same, but the mixing and baseband stages are digital by directly sampling the RF from the antenna after amplification and filtering.

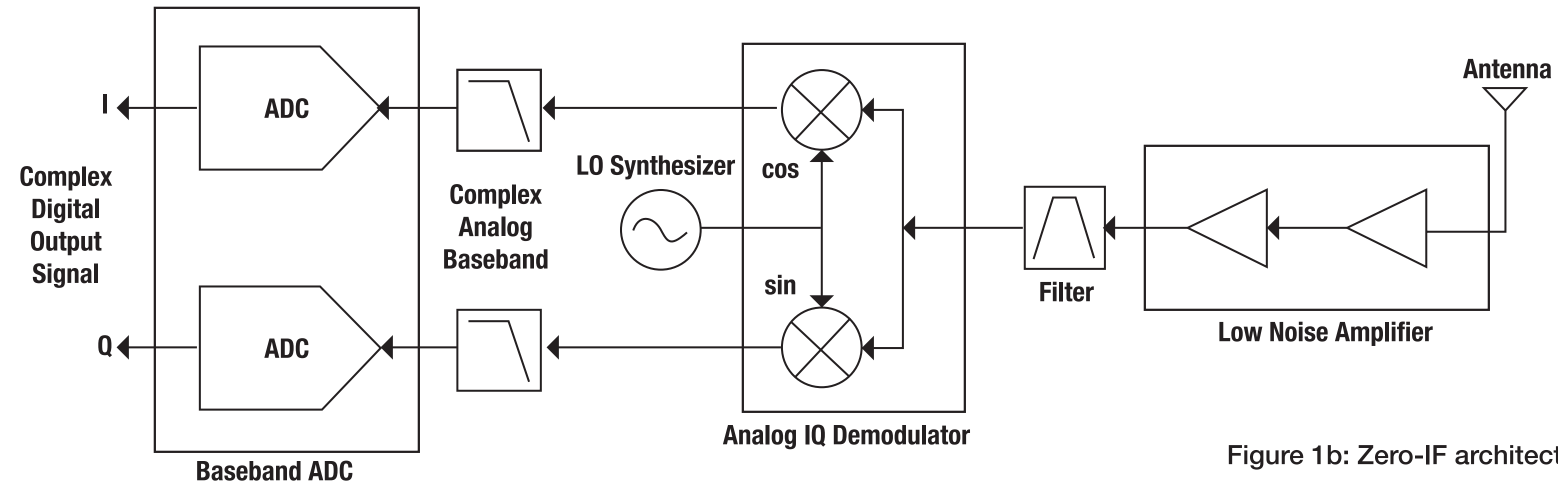


Figure 1b: Zero-IF architecture.

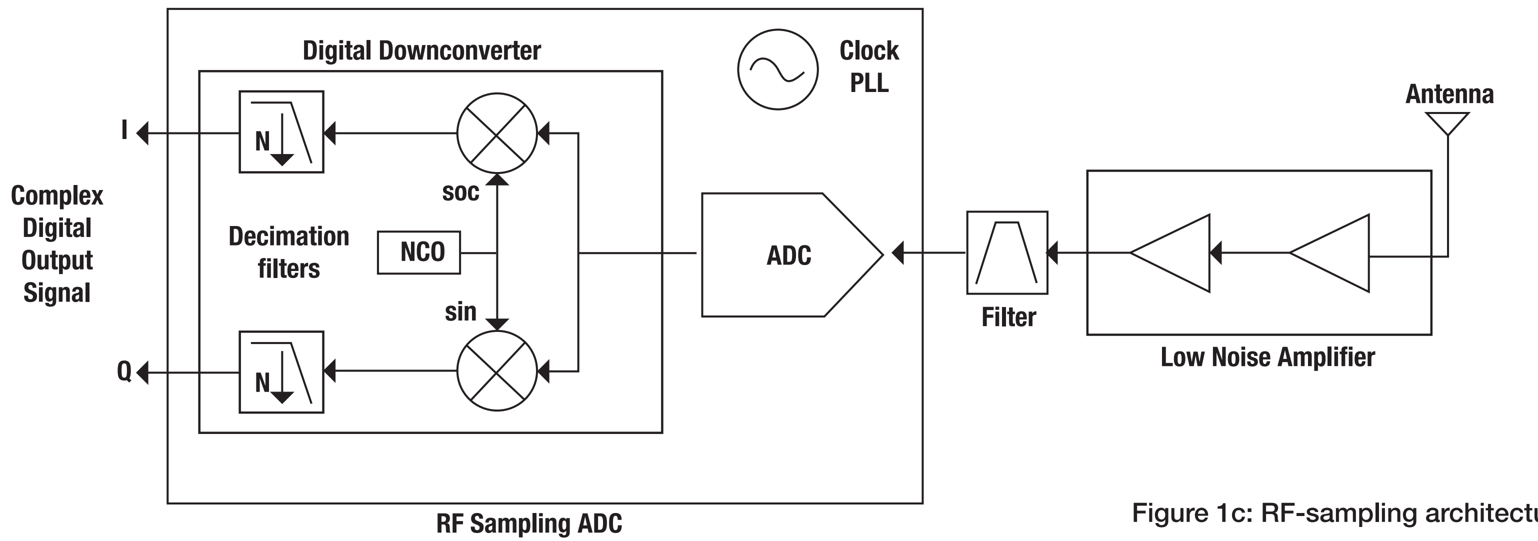


Figure 1c: RF-sampling architecture.

Adding a second band in an IF or zero-IF architecture typically requires a second signal chain with additional components because of bandwidth limitations. By comparison, RF-sampling ADCs run at multi-gigasample-per-second speeds and can digitize wide bandwidths at RF, covering multiple cellular bands with one ADC. In this case, adding two or more bands requires only additional digital down-converters to convert the additional bands to baseband signals.

Of course, RF sampling would not be attractive if the performance and power dissipation were worse than the IF or zero-IF architectures. As complementary metal-oxide semiconductor (CMOS) process technology has increased the speed and lowered the power of digital circuits, RF-sampling ADCs now have similar performance at lower power than traditional architectures.

Table 1 compares IF, zero-IF, and RF-sampling architectures for a four-receiver (RX) system with 100 MHz of bandwidth per band. The traditional architecture comprises the Texas Instruments TRF37B32, LMH6521, ADC16DX370, and LMX2581. The values taken from the TSW16DX-370EVM evaluation module are described in the User's Guide.

For zero-IF, I use the RX-mode specifications from a commercially available dual channel integrated transceiver, and for RF sampling, I use the RX side of the AFE7686, a quad-channel transceiver with 9-GS/s RF DACs and 3-GS/s RF ADCs. I used several key performance parameters at 2.6 GHz as a benchmark.

Starting with size for a single band, one RF-sampling analog front end (AFE) and two dual-channel zero-IF transceivers are roughly the same size, while the discrete IF architecture is 10 times larger. Power for the zero-IF transceiver is 28% lower but, as discussed below, with a lower performance in the presence of large interfering signals.

For a dual-band system, you can use the same RF-sampling AFE with a minimal increase in power. For IF and zero-IF architectures, the component count, size, and power all double. The advantages are even larger when adding a third or fourth band.

Parameter	IF	Zero-IF	RF sampling
Single-band system			
No. of active components	7	2	1
Size	2x 60mm x 40mm	2x 12mm x 12mm	17mm x 17mm
Power dissipation	8.5W	5.4W	7.5W
Dual-band system			
No. of active components	14	4	1
Size	4x 60mm x 40mm	4x 12mm x 12mm	17mm x 17mm
Power dissipation (Four RX channels)	17W	10.8W	7.5W
Specifications (maximum gain)			
Noise figure	11dB	13dB	19dB
IIP3	7dBm	22dBm	23dBm
IIP2	Not applicable[1]	45dBm	Not applicable[1]
In-band SDFR	83dBc	73dBc	80dBc
Sideband image (adjusted)	No image	75dBc	No image
LO feedthrough	No feedthrough[2]	-85dBFS	No LO
Phase-locked loop phase noise (1MHz offset)	-135dBc/Hz	-123dBc/Hz	-126.7dBc/Hz
Dual-band gain control	Yes	Yes	Single dynamic spectrum access for both bands

[1]Second-order distortion product does not fall in band
[2]LO feedthrough falls out of band

Table 1: Architecture comparison for a quad receiver at 2.6 GHz.

Looking at the performance specifications, RF sampling has a somewhat higher noise figure than the IF or zero-IF examples. As a result, the low-noise amplifier needs more gain before the RF-sampling AFE to reduce the overall system noise figure. To receive small wanted signals in the presence of a large interfering signal, the RF-sampling AFE performance exceeds zero-IF receiver performance because of the latter's worse in-band spurious free dynamic range (SFDR) and sideband image. However, the discrete IF architecture has several advantages — SFDR and phase noise — that could provide the best in-band dynamic range. Another benefit is that you can use a sharp IF filter, like a surface acoustic-wave filter, to significantly suppress out-of-band interfering signals.

One final difference: For multiband RF sampling, the integrated digital step attenuator at the input simultaneously controls the input level for all bands, although it is possible to use separate external variable gain amplifiers for each band. The presence of a large interfering signal in one band that requires an increase in attenuation will affect the system noise for the other band, reducing the sensitivity level. With two separate single-band receivers, you can independently control the gain for each band so that an interferer in one band does not affect the sensitivity in another band.

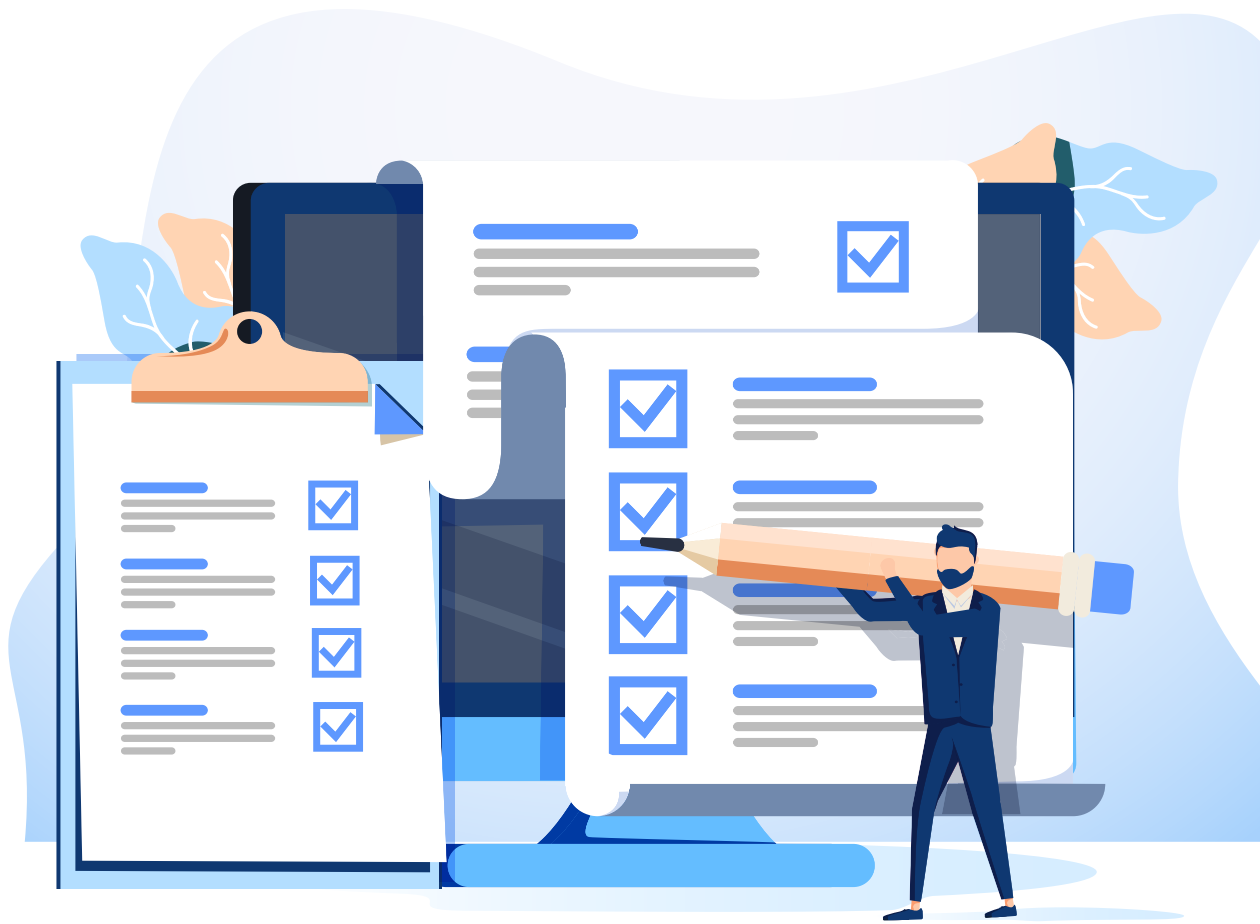
As demonstrated here, RF sampling has emerged as a new, competitive architecture for cellular infrastructure applications.

A Checklist for Designing RF-Sampling Receivers

By Thomas Neu, *System Engineer, Texas Instruments*

The modern, advanced CMOS direct radio frequency (RF)-sampling data converter has been eagerly awaited by system design engineers for several major end-equipment manufacturers. This includes manufacturers of communications infrastructure, software-defined radios (SDRs), radar systems, or test and measurement products. Recently introduced data converters are delivering the high dynamic range comparable to high-performance intermediate frequency (IF)-sampling data converters. Additionally, these converters integrate on-chip digital filtering (DDC), which reduces the output data rate from a 3- to 4-GS/s sampling rate to something more manageable and similar to traditional IF-sampling data converters.

Two major factors are driving the quick adoption of these ultra-high-speed data converters. The ever-increasing demand for wider bandwidth naturally requires faster sampling rates, while higher density and integration is



accomplished by removing one down-conversion stage from the receiver, for example. Modern SDRs or cellular base stations need to be able to cover multiple frequency bands simultaneously, for example, to support carrier aggregation across multiple licensed Long-Term Evolution (LTE) bands to enable faster data traffic. Rather than expending one radio-per-band system, designers want to shrink the product form factor and build a multiband-capable radio. The RF sampling data converter removes the IF stage, saving printed circuit board (PCB) area and power consumption, while its wide Nyquist zone enables sampling multiple bands simultaneously.

System designers who are considering switching from IF sampling to RF sampling need to solve four primary challenges on their checklist:

1. Receiver sensitivity
2. Radio performance in presence of in-band interferer
3. Filter requirements for out-of-band blocker
4. Performance of the sampling clock source

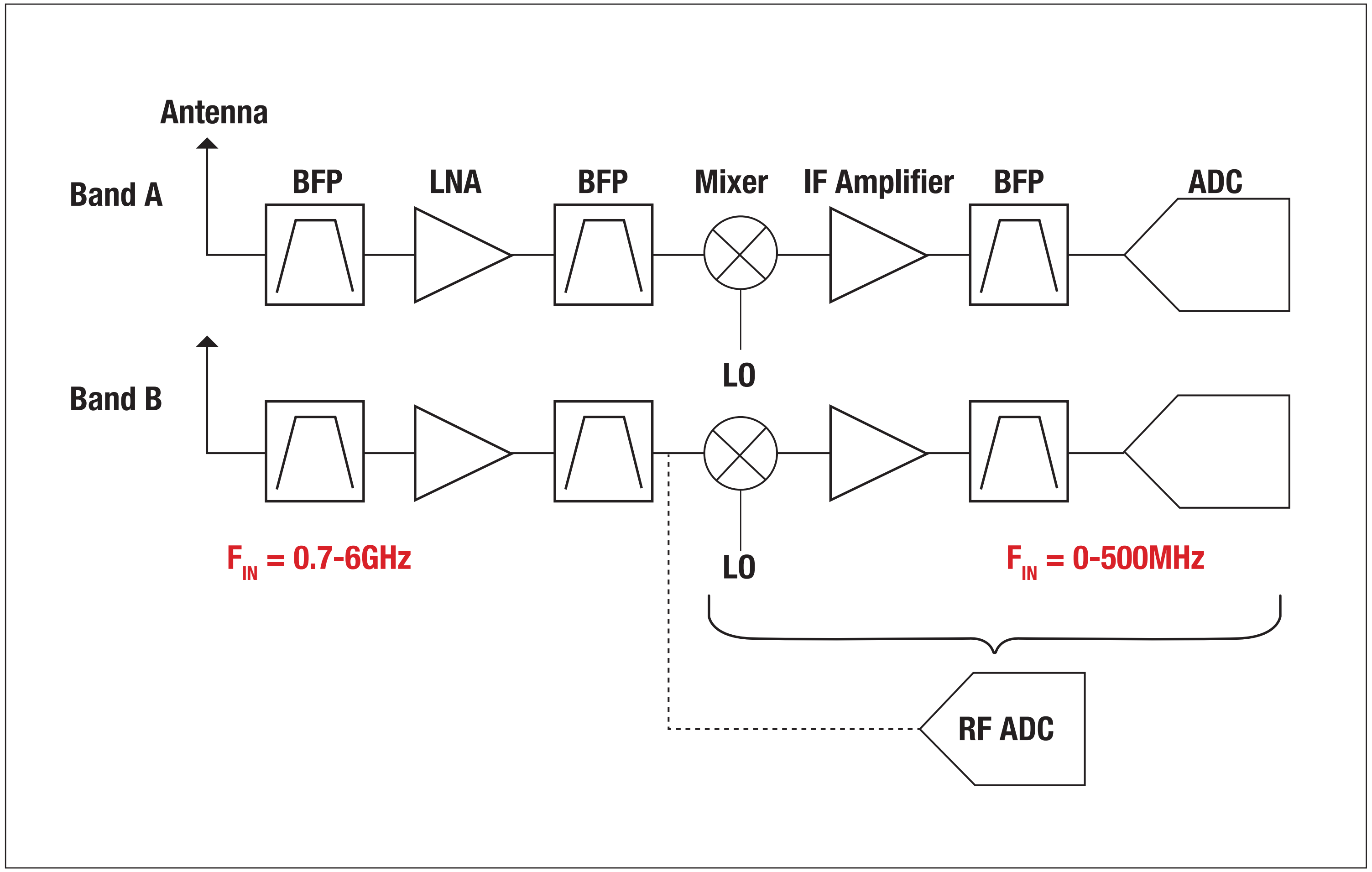


Figure 1: One RF-sampling ADC can replace multiple IF-sampling signal chains.

Depending on their application, some may be more critical than others.

Let us examine these challenges using two different types of analog-to-digital converters (ADCs) and compare the results. The first data converter is the ADS4249, a14-bit, 250-MS/s ADC used for an IF-sampling system. The second is the ADC32RF45, a 14-bit, 3-GS/s ADC for an RF-sampling system.

Receiver sensitivity

One basic performance metric of the receiver is its sensitivity, or the weakest signal power that it can successfully recover and process. Weak input signals cannot be demodulated if the noise of the receiver within the demodulated bandwidth is larger than the received signal itself. The noise floor of the receiver is typically expressed as a noise figure (NF) in decibels (dB), or the difference to the absolute thermal noise normalized to 1-Hz bandwidth. The most common way to improve an ADC's noise figure is to add an amplifier before the ADC.

The noise figures of the IF- and RF-sampling converters can be calculated as shown in **Table 1**.

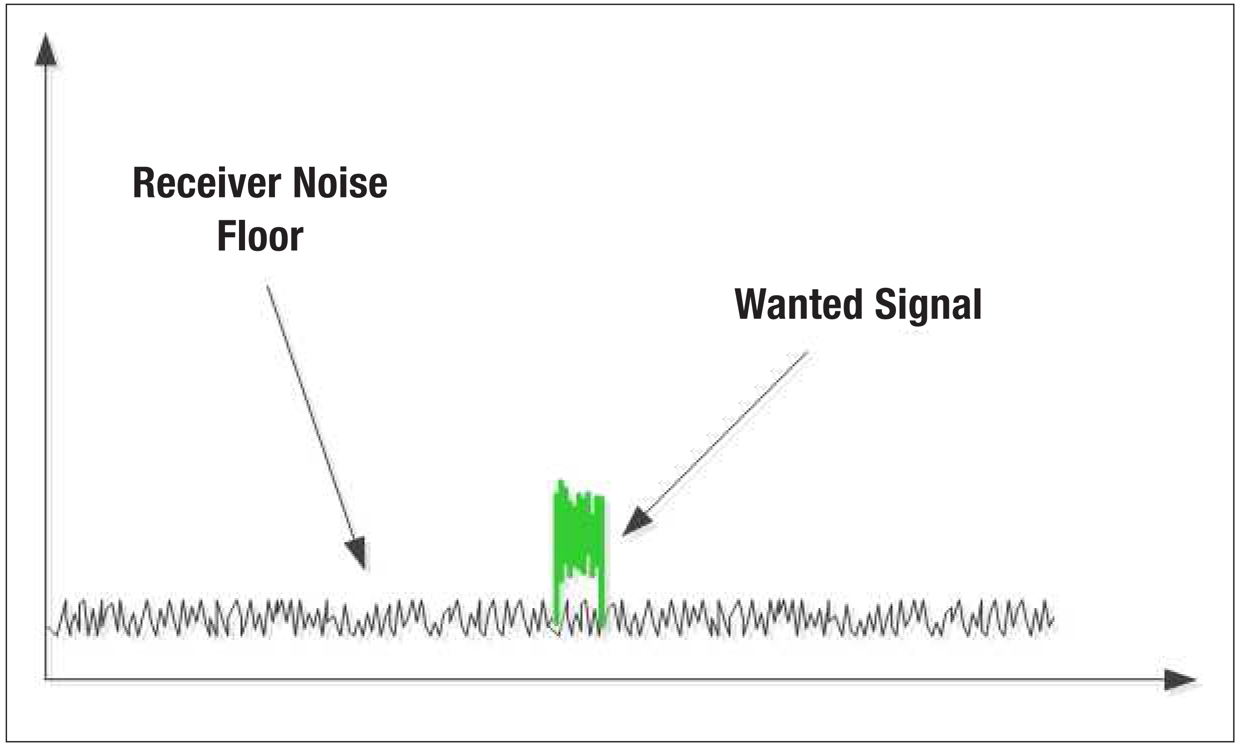


Figure 2: Small wanted signal in sensitivity case.

Parameter	IF sampling ADC	RF sampling ADC
Sampling rate (FS)	250 MSPS	3 GSPS
Input full-scale (V_{pp})	2 V_{pp}	1.35 V_{pp}
Thermal noise	72.8 dB	62 dB
Input impedance (Zin)	200 Ω (external)	50 Ω (internal
Calculated noise figure	**24.2 dB**	**26.8 dB**

Table 1: Noise figure comparison between IF- and RF-sampling data converters.

While the noise figures of both converters are close, the IF-sampling data converter has significant external gain from the mixer and IF digital variable gain amplifier (DVGA), which substantially reduces the impact of the ADC noise figure to the receiver sensitivity. Hence, the RF-sampling ADC requires additional front-end gain (an additional low-noise amplifier, or LNA) to minimize its impact on receiver sensitivity as well.

Parameter	IF sampling ADC F_{IN} = 170 MHz	RF sampling ADC F_{IN} = 1.8 GHz
HD2, typ	80 dBc	63 dBc
HD3, typ	80 dBc	67 dBc
Non HD2, 3typ	80 dBc	80-85 dB

Table 2: Spurious-free dynamic range performance of both IF- and RF-sampling data converters.

In-band blocking performance

Sometimes, interferers manage to get within the front-end filter passband. The receiver in-band blocking performance is a measure of how well the receiver can demodulate weak signals in the presence of such an in-band interferer. The automatic gain control (AGC) of the receiver ensures that the interferer power level stays below the ADC input full-scale to avoid saturation. However, the blocker harmonics generated inside the ADC during the sampling process can still fall on top of the weak wanted signals, reducing the receiver's ability to demodulate.

Because the input frequency is much lower, the IF-sampling data converter offers substantially better low-order harmonic (such as HD2,3) performance, as shown in **Table 2**.

However, system designers are taking advantage of the high sampling rate of RF-sampling converters. Designers can select either the input frequency range (for example, military SDR operating in the L-band) or the sampling clock frequency (such as communications infrastructure with fixed-RF frequency bands) to avoid low-order harmonics to fall in-band. The high-order distortion performance of modern RF-sampling converters is comparable to that of high-performance IF-sampling converters. This method is also known as frequency planning.

The frequency-planning concept is illustrated in **Figure 3**. A 60-MHz-wide spectrum is centered at an IF of 180 MHz with a 250-MS/s ADC. The harmonics of the in-band interferer cannot be avoided. By contrast, the same 60 MHz centered at 1.75 GHz sampled at 3 GS/s provides in-band spurious-free dynamic range (SFDR) that is free of low-order harmonics and interleaving spurs (**Figure 4**).

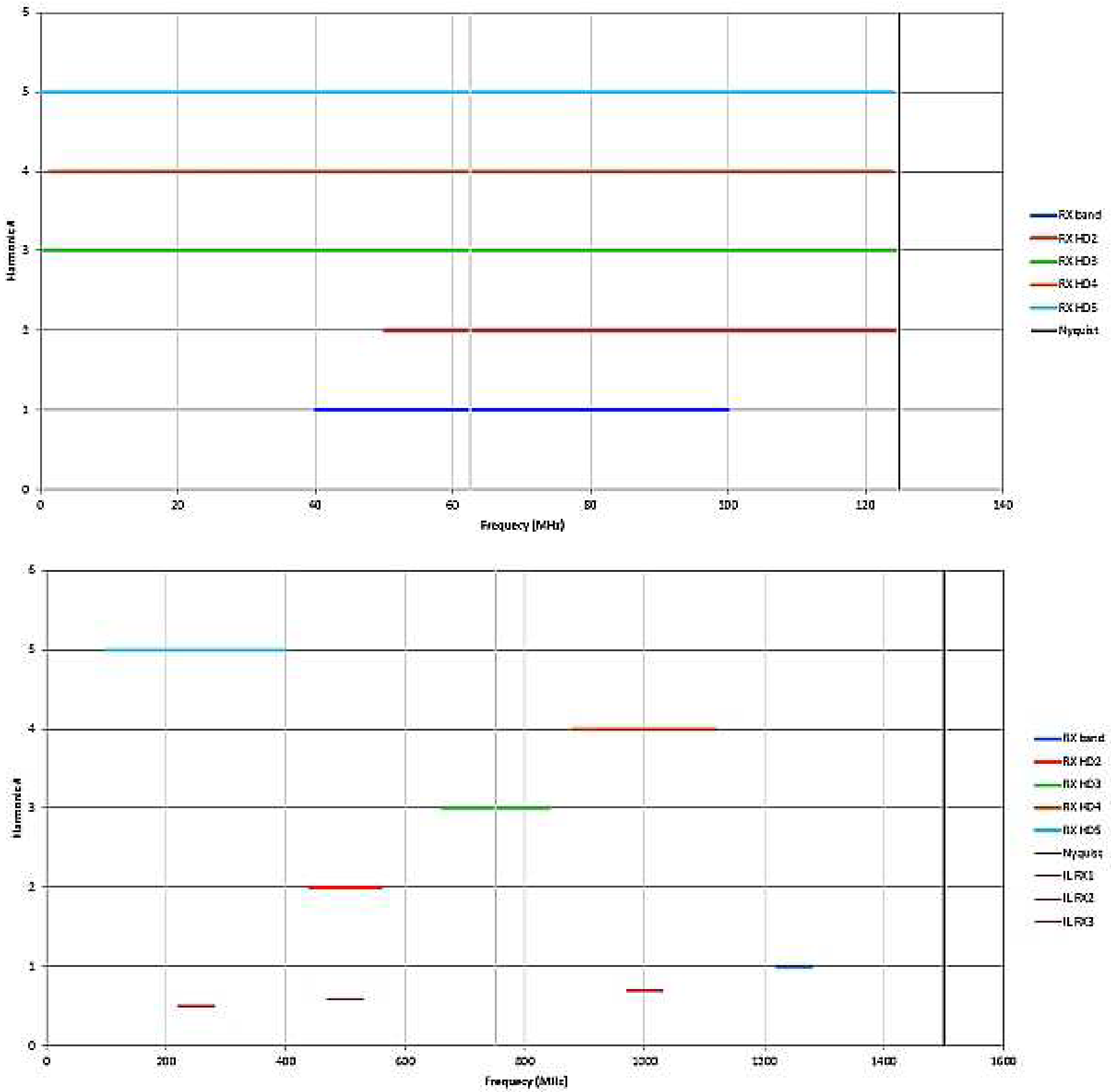


Figure 3: Frequency spectrum of 60-MHz bandwidth with IF sampling (Fs = 250 MS/s centered at 180 MHz) (a) versus RF sampling (Fs = 3 GS/s centered at 1,750 MHz) (b).

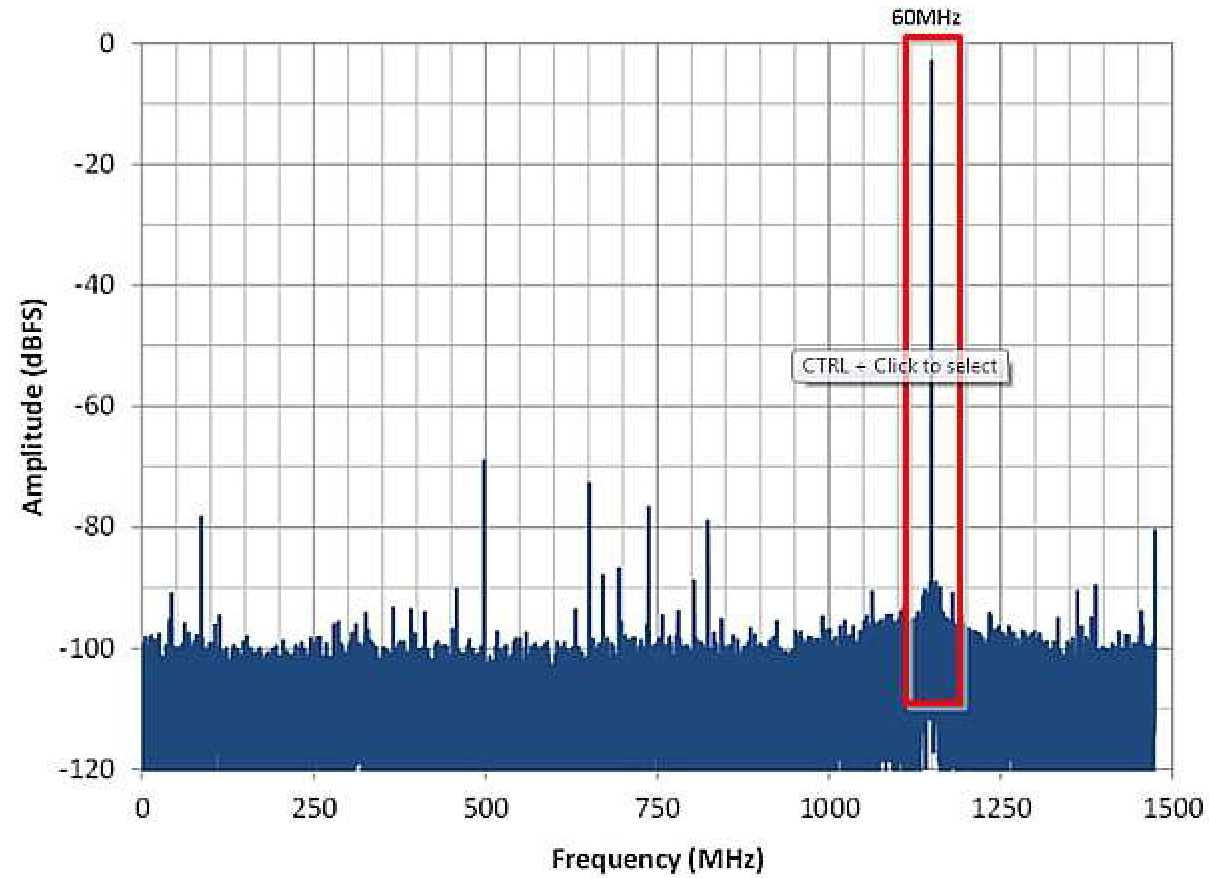


Figure 4: FFT plot of an ADC, Fs = 3 GS/s, F_{IN} = 1.75 GHz.

External blocker filter requirements

Independent of architecture, the ADC input must be protected from large, out-of-band interferers because that would either alias the in-band to exceed the ADC full scale and saturate the receiver or generate harmonics that would overlap with a small, in-band wanted signal.

Intermediate frequency-sampling systems have a relatively small Nyquist zone; therefore, the alias bands and mixing images are fairly close by. Because it is difficult to design an RF filter with sharp rolloff, the filter attenuation is typically split between RF and IF bandpass filters.

The filter design for RF-sampling systems is a little bit more relaxed when frequency planning is applied. There are no mixer images or LO spurs to worry about, but low-order harmonics, or interleaving spurs of out-of-band interferers, still need to be considered.

Sampling clocking performance requirement

The sampling clock for the RF ADC is equivalent to the local oscillator in a heterodyne receiver. Clock phase noise requirements are highly dependent on the application. Generally, it is better to specify the phase noise at application-specific offset frequencies versus integrating the clock phase noise across the entire (rather large) Nyquist zone for a representative clock jitter number.

Furthermore, the clock is now an RF signal and faces additional challenges, such as increased amplitude attenuation with increased frequency. ADCs require clock amplitude to be as high as possible for the lowest noise floor and tough skew management in multi-channel systems.

Similar to suitable RF- and IF-sampling ADCs, there are fewer high-quality, low-phase-noise clocking solutions available for clock rates above 1 GS/s. Therefore, system designers may need to rely on using low-phase noise LOs, such as the LMX2582, as the RF ADC clock source.

Summary

The availability of high-dynamic-range RF-sampling converters, such as the ADC32RF45, enables direct RF-sampling receiver implementations for a wide range of applications. When transitioning from a traditional heterodyne design to a direct RF conversion, the designer should not have to compromise on radio performance. However, attention still needs to be given to the four major design challenges discussed in this article.

References

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- Keller, Robert. Signal chain basics #45: Is high-speed ADC clock jitter being over-specified for communication systems?. Planet Analog. Sept. 2, 2010.

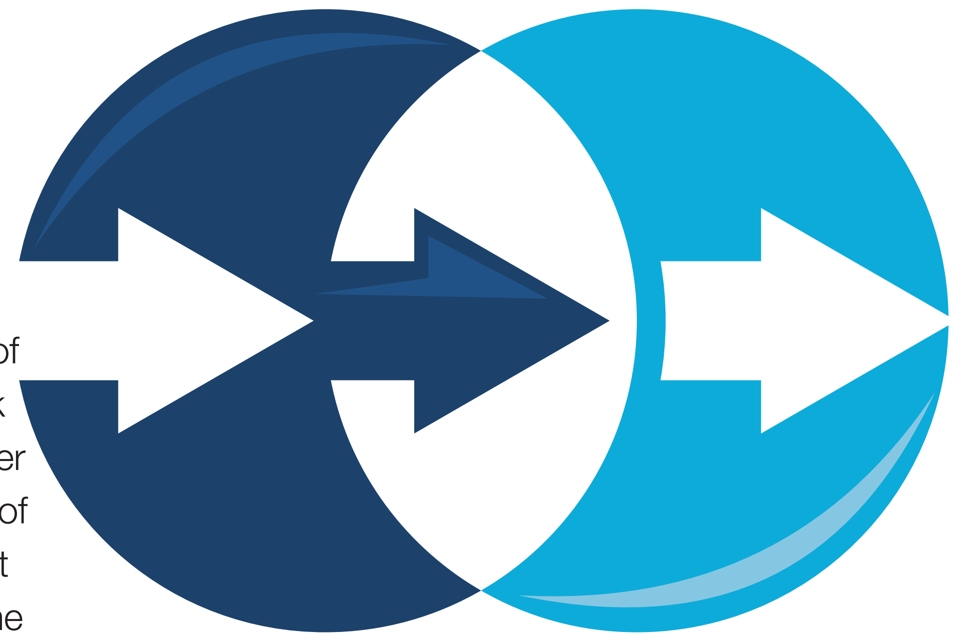
Designing Higher-Frequency Active Filters to Drive Differential Input High-Speed ADCs

By Michael Steffes, *Senior Applications Manager, Intersil Corp.*

With newer-precision fully differential amplifiers (FDAs) providing more than 800-MHz gain bandwidth (GBW) product, the available frequency range for active filter designs combined into the last stage interface to an ADC have moved beyond what legacy literature would suggest. Steadily improving amplifier choices and RC value adjustment routines for GBW have increased the frequency application range for these active filters. A recent >30-MHz active filter design will be described here and updated to more accurately fit the desired response shape.

Example design driving a low-power, quad-channel, 12-bit, 50-MS/s ADC

A complete design incorporating a JFET input stage into a fourth-order single to differential stage using the THS4541[1] FDA can be found in a recent (2016) reference design.[2] One final iteration (Section 8, Ref. 2) added another pair of poles into the FDA stage as a multiple feedback (MFB) active filter prior to a passive second-order RLC filter at the ADC inputs. These two stages of second-order filters were intended to implement a fourth-order Bessel filter at 20 MHz (F_{-3dB}). One source for the filter targets can be found in the



Intersil filter designer.[3] Here, we need only the Fo and Q for each of the second-order filter stages, as shown in **Figure 1**. This tool appears to be the only extant vendor tool supporting frequencies this high in an active filter implementation, although there are no FDAs in this (or any) vendor tool.

The first pair of poles were easily added to the THS4541 FDA single to differential stage as an MFB filter design. The second pair is implemented as a passive differential RLC filter at the ADC inputs. **Figure 2** shows the TINA[4] simulation circuit for this original design. At the time of this design, a standard RC value selection was not employed — that step will be added here as well.

This overall low-pass filter was intended to be DC attenuating with 20-MHz F_{-3dB}. The simulation shows this to be slightly off, at about 20.9 MHz. Benchtesting this single-ended JFET input to differential ADC driver with this fourth-order filter showed the excellent performance of **Figure 3**.

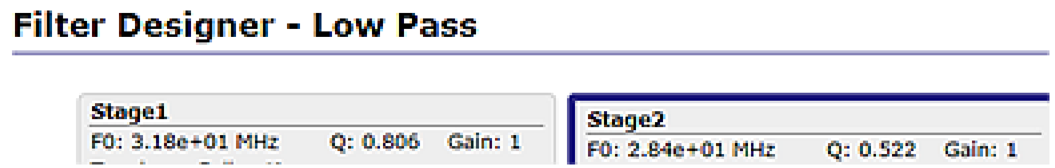


Figure 1: Filter stage targets from the Intersil Active Filter Designer.[3]

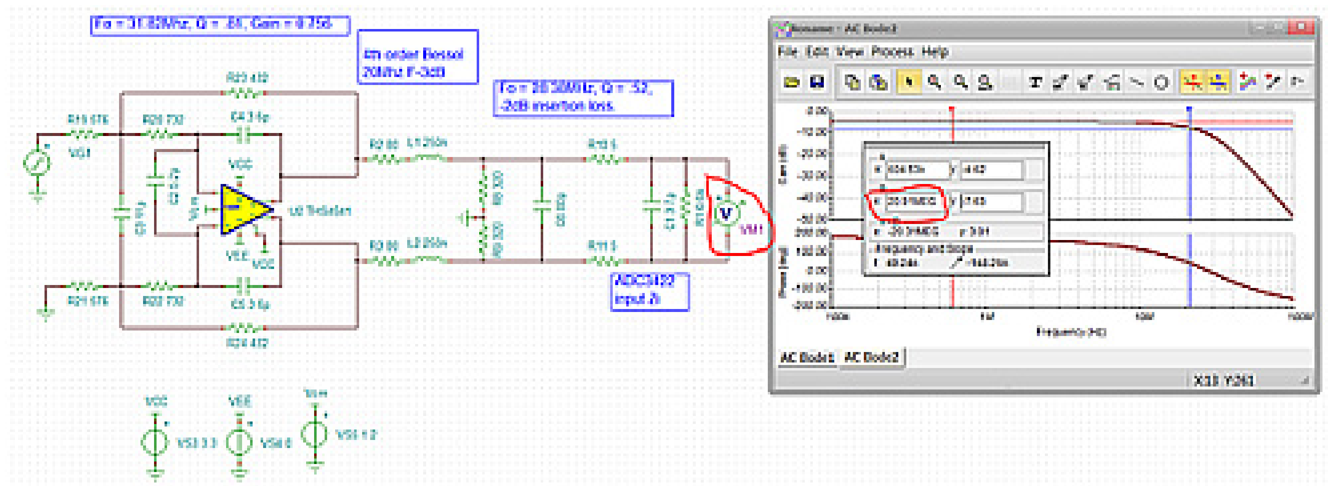


Figure 2: Original fourth-order Besse design simulated to ADC inputs (Ref. 2, Page 20)

Testing the response fit for the active filter stage

The small signal response for the active filter stage can be simulated and compared to the ideal target. One nuance moving the response off target is the differential input capacitance (C2, **Figure 2**) used to im prove the phase margin in this design. The THS4541 is not unity-gain–stable (**Figure 1**, Reference 1), and this capacitor transitions the AC noise gain to a higher level at loop gain x-over (Reference 5). The high-frequency noise gain in **Figure 2** is set by the input differential capacitance (doubled

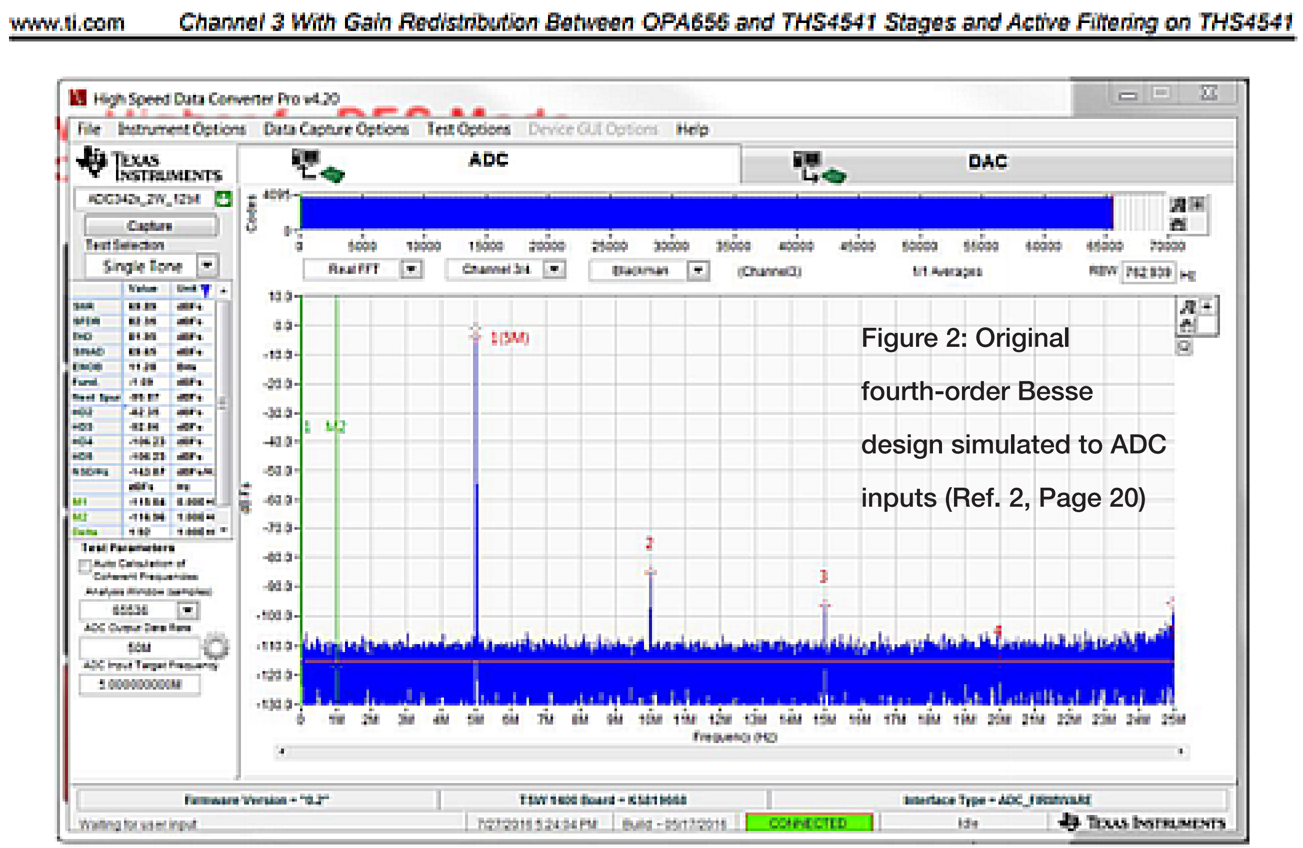


Figure 3: Full-scale 5-MHz input FFT for original circuit + ADC showing 69.9-dB SNR and 82-dB THD

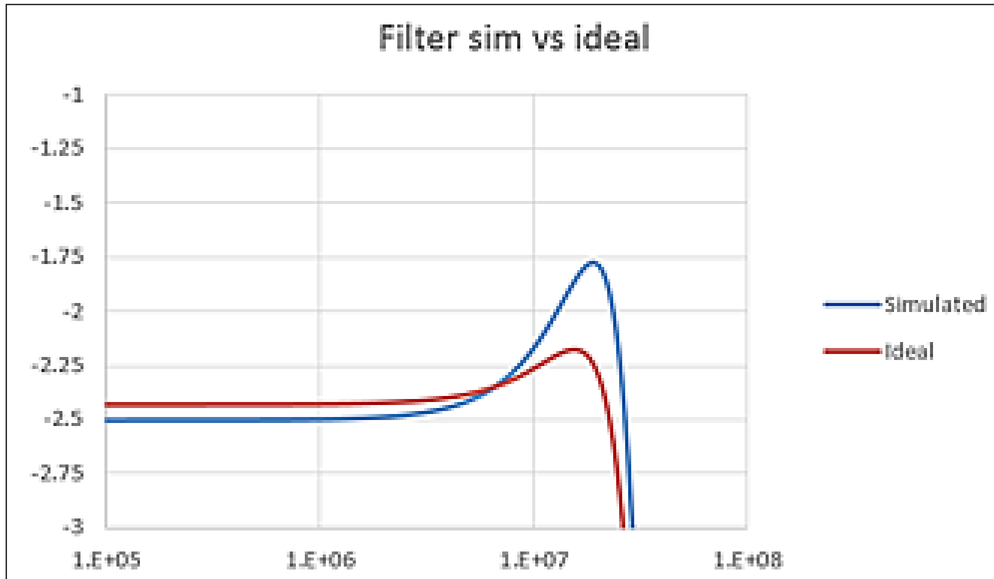


Figure 4: FDA filter stage response versus ideal target.

to make it single-ended) divided by the feedback capacitance (1+(2*5.2 pF)/3.6 pF = 3.9 V/V). This higher noise gain (to improve phase margin) effectively reduces the 850-MHz GBW of the THS4541 to 218 MHz in a 31-MHz active filter implementation. This modest GBW margin would definitely suggest that a GBW RC adjusted flow might be useful. Measuring the simulated response at the output of the FDA in **Figure 2** (keeping the RLC filter load in place) and comparing to the ideal response gives **Figure 4**.

The higher peaking (Q) than targeted can explain the higher overall F_{-3dB} bandwidth than intended. This original design was producing an F_{-3dB} at 36.6 MHz versus the

	Target numbers	Simulated frequencies				Target peaking (dB)
Fpeak ==>	1.5524E+07 Hz	1.9011E+07 Hz		Linear peaking ->	1.0871816	
F-3dB ==>	3.5727E+07 Hz	3.6559E+07 Hz		dB of peaking ==>	0.7260419 dB	2.53E-01 dB
		Fo est. from Fpeak	3.03E+07 Hz	Low F gain ==	-2.4987472 dB	
		Fo est. from F-3dB	3.02E+07 Hz	Linear low F gain ==>	0.75000238 V/V	
		Avg Fo from sim	3.03E+07	Target F-3dB ==>	-5.5087472	
		Target FO	3.18E+07	Simulated Q	9.07E-01	
		%error	-4.87%	Target Q	8.10E-01	
				% error	11.99%	
				(1-1/(2Q^2)->	0.3923652	

Figure 5: Extracted closeness of fit on F_o and Q.

intended 35.7 MHz. Extracting the simulated response details and comparing to the intended design shows the large fit errors in **Figure 5**.

Improving the MFB stage design adjusting the RC values for GBW

The design of **Figure 2** was done without applying a more sophisticated GBW adjust flow on the RC values. This flow, using a cubic pole expression including the amplifier GBW (Reference 6), can be effectively applied here to fine-tune the RC values, possibly improving the fit to target. As noted in Reference 6, including an op-amp summing junction noise gain tuning capacitor in the cubic polynomial coefficients is possible without changing the order of the transfer function. That would be necessary here to apply a non-unity gain stable FDA. **Figure 6** shows the slightly modified RC values that will give a much closer fit in this relatively high-frequency design.

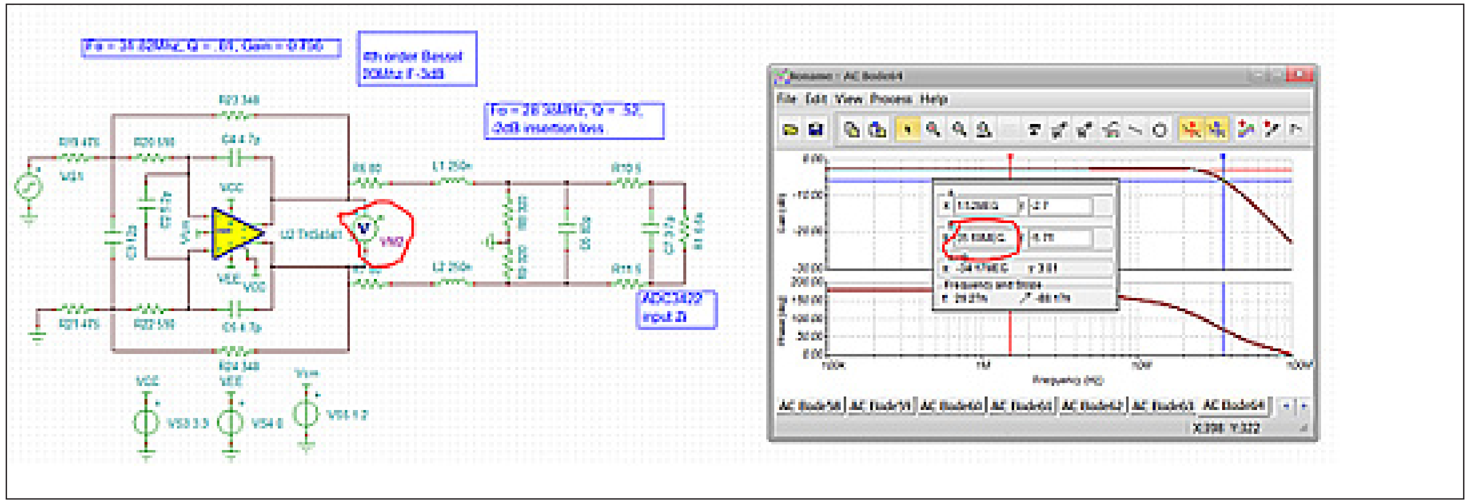


Figure 6: Modified RC values in the THS4541 active filter stage to adjust for GBW and C2.

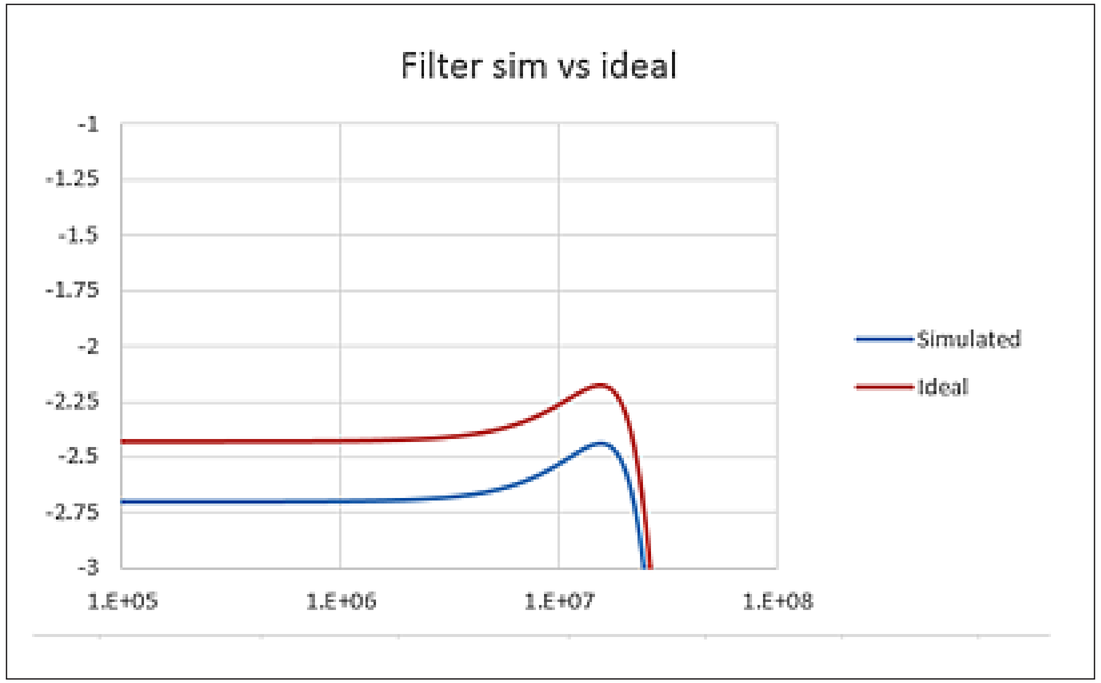


Figure 7: Updated MFB filter design response versus ideal.

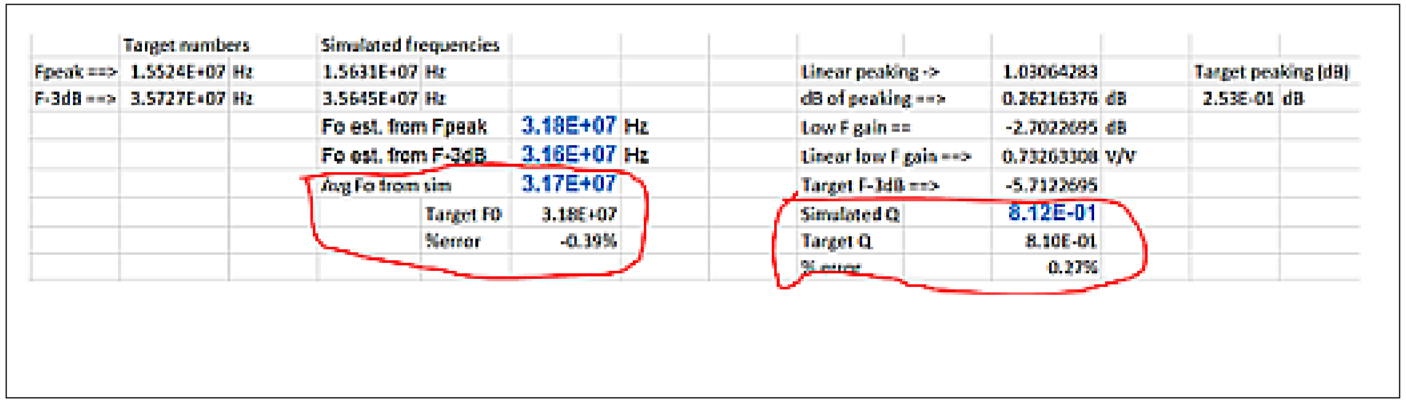


Figure 8: Fit errors using a GBW adjusted RC design flow.

Putting these RC values into an ideal op-amp second-order MFB response extraction will appear to be mistargeted. However, **Figure 7** shows that these are adjusting very successfully for the THS4541 850-MHz GBW and the 5.2-pF C2 across the FDA input pins.

The best fit RC standard-value algorithm used here focused only on F_O and Q fit and allows the DC gain to go off 1 – E96 resistor step value if that improves the filter fit. The DC gain can usually be adjusted back to target in another stage — like the input JFET stage used in this reference design.[2] Extracting the closeness of fit parameters shows the improvements in **Figure 8** (compare to **Figure 5**). The 35.69 MHz = F_{-3dB} has moved much closer to the intended 35.73 MHz.

To complete this redesign for closer fit, also adjust the RLC filter to standard values and back out the ADC input capacitance from the final differential C — taking it down from the exact 80-pF solution to the next 75-pF standard value. Simulating this completed redesign shows the much closer nominal fit at 20.35 MHz versus the targeted 20-MHz F_{-3dB}, only adjusting RC values in this fourth-order active and passive filter solution.

The example RC values developed here should also work well with the similar ADA4932-1 from ADI.[8]

Modern high-speed voltage feedback op-amps and FDAs can deliver higher-frequency active filter solutions than commonly assumed. The only tool currently supporting a GBW adjusted flow appears to be the ADI Filter Wizard.[7] Some of the features that appear to be missing from all the current vendor tools include the following:

1. No attenuating MFB filter designs are allowed — but physically easy to implement.

2. FDAs are not directly supported (FilterPro[9] does show designs but only for an ideal FDA).

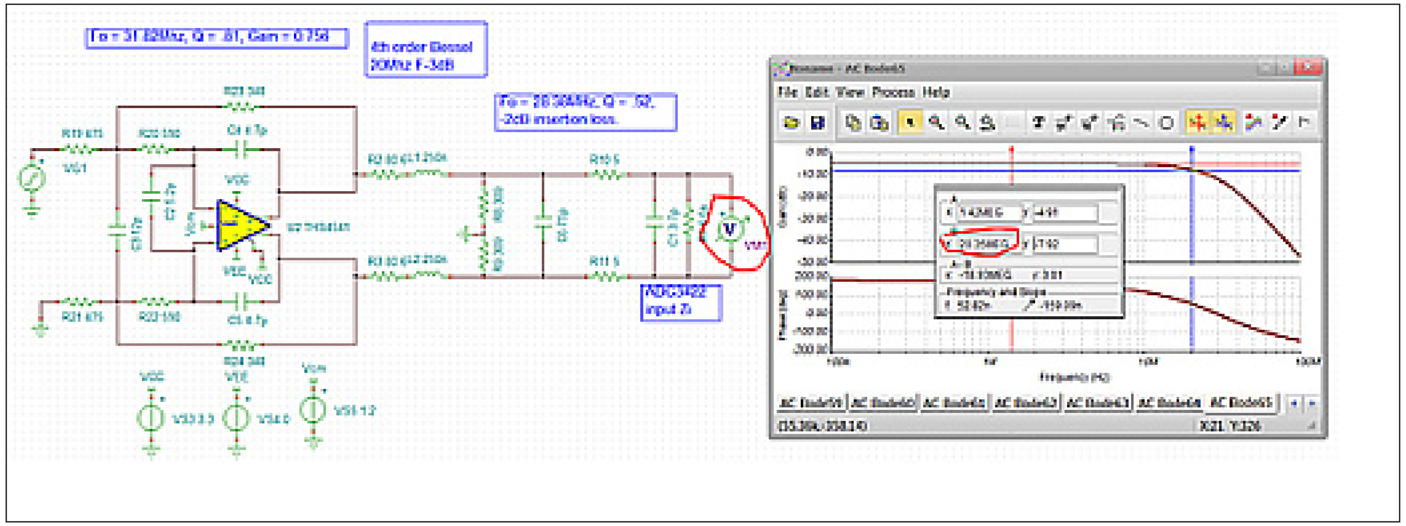


Figure 9: Updated design with standard values and improved design fit.

3. Noise gain tuning with a capacitor on the summing junction(s) for phase margin improvement is not directly supported. It can be added as a final step, but that will interact with the response shape if not initially included in the GBW RC adjusted value flow.

4. The allowed design frequencies are lower than possible with today's higher-speed devices. The ADI Filter Wizard delivers buffered RLC designs if asked for this solution. TI's WEBENCH Active Filter Designer[10] constrains frequency entries to a maximum 10 MHz.

Modifying channel 3 in the reference design[2] to the improved RC values shown here would slightly improve the step response, as the initial design was overshooting more than expected out of the active filter stage.

Even though these new RC values provide a slight improvement, they will deliver a much better nominal fit to target whereas the next step would be to run RC tolerance Monte Carlo to get the response spread around this more centered nominal. The ADI tool[7] also supports this feature but not with FDAs nor in this frequency range. Lower-frequency designs using an op-amp of the same GBW as the intended FDA can certainly take advantage of the GBW adjust and Monte Carlo spread features in the ADI tool. The op-amp design could then be easily adapted to an FDA version using a device with similar GBW.

Improved THS4541 active filter references

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2. TI Designs TIDA-00799, Quad-Channel, 12-bit, 50-MSPS ADC Reference Design with Low-Noise, Low-Distortion, DC and AC Inputs.
3. Entry page for the Intersil online op-amp design tools. Login required.
4. TINA simulator available from DesignSoft for <$350 for the Basic Plus edition. Includes a wide range of vendor op-amps and FDAs and is the standard platform for TI op-amp models.
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