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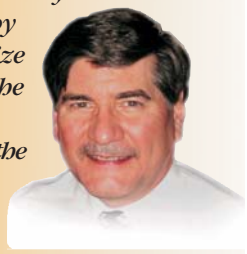
In This Issue

- **Communication systems** requirements and how they are met with FPGAs on mezzanines is the topic in this issue's feature article. More in the feature article.

"New technologies and mezzanine standards have cast mezzanines for communication systems into complex and critical roles previously handled by other full-size boards in the system. Choosing the right mezzanines now is a much more significant part of a successful system design."



Rodger Hosking, Pentek Vice President and Cofounder

- **Product Focus:** Model 6890 Sync and Gate Distribution board Click here
- **Product Focus:** Model 7140-420 Gateflow Transceiver Click here

Technical Resources

Download the 6th edition of the *Digital Receiver Handbook:*
pentek.com/go/pipedrhb

Download the 3rd Edition of *FPGAs for Software Radio Handbook:*
pentek.com/go/pipefpgahb

Download the 2nd Edition of *Critical Techniques for High-Speed A/D Converters in Real-Time Systems Handbook:*
pentek.com/go/pipehshb

Mezzanine Board Strategies for Communication Systems

Few embedded system applications encompass a more diverse range of frequencies, numbers of channels, data rates, signaling schemes, and signal processing algorithms than communications systems. Apart from this extreme diversity, communication systems must now handle wider signal bandwidths to meet the needs of new complex modulation schemes and higher data rates to support large numbers of channels.

System integrators faced with the task of delivering custom communication systems using COTS board-level products have traditionally relied on mezzanine boards, also known as daughter cards, for modular and flexible interfaces. However, new technologies and mezzanine standards have cast mezzanines for communication systems into complex and critical roles previously handled by other full-size boards in the system. By cutting costs and boosting performance, choosing the right mezzanine boards now becomes a much more significant part of a successful system design.

Communication System Basics

As shown in Figure 1, the receive section of a modern communication system typically starts with an analog RF stage that amplifies and downconverts the antenna signal to an IF frequency. This IF signal can then be digitized by a wide range of monolithic A/D converters capable of 14- or 16-bit accuracy and sampling frequencies of 100 MHz and higher. The IF signal bandwidth usually covers the entire span of the particular communication band and may contain many different carriers, each at its own frequency.

In order to extract multiple signal channels from this digitized IF band, a digital downconverter (DDC) is required. This process, in turn, starts with a digital local oscillator that produces samples of a sine wave set to the carrier frequency. The samples from the A/D are then mixed with the oscillator samples using a digital multiplier. This translates the carrier signal down to baseband and produces a complex (I+Q) digital signal with upper and lower sidebands centered at 0 Hz. A digital low pass filter, set for the signal bandwidth, removes adjacent channel signals leaving only the channel of interest. Because the bandwidth of the filtered output has been reduced, an output decimator drops the sampling rate commensurate with that bandwidth. ➤

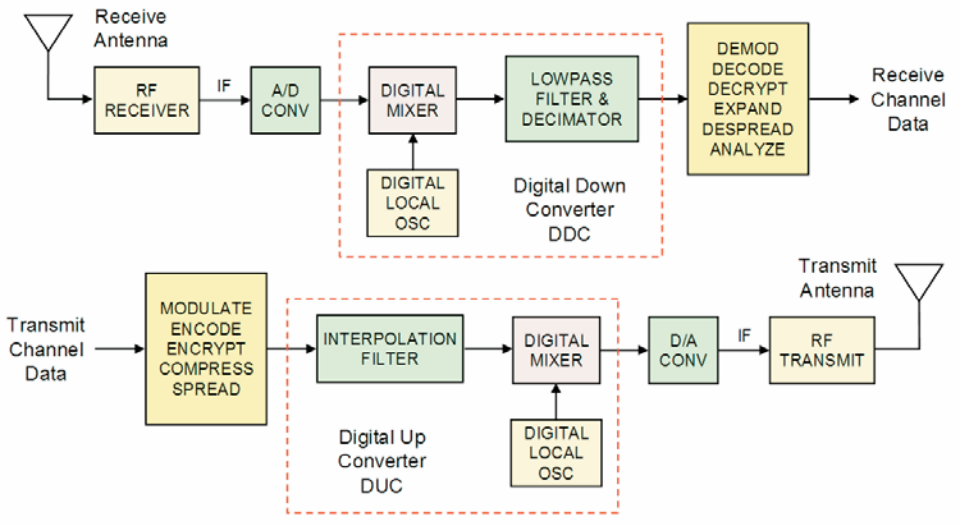


Figure 1. Signal-processing Blocks of a Typical Communications Transceiver System

Mezzanine Board Strategies for Communication Systems

➤ Finally, depending on the type of transmission employed, additional processing steps for demodulating, decoding and decrypting are needed to recover the receive channel data. All of the digital signal processing steps shown in the top half of Figure 1 to the right of the A/D must be repeated for each channel.

On the transmit side, the signal processing steps are exactly reversed, as shown in the lower half of Figure 1. Transmit channel data must first be processed with the appropriate modulation, encoding and encryption to make it compatible with the transmission channel protocols. The digital upconverter (DUC) stage then follows. Here, the digital sample stream signal enters an interpolation filter that preserves the frequency characteristics of the signal, but boosts the sampling rate to match that of the digital mixer and local oscillator. These stages upconvert the baseband transmit signal to the IF frequency. A D/A converter produces an analog IF signal, which is fed into the analog RF transmit section to drive the antenna. All the signal processing steps to the left of the D/A must be repeated for each channel.

Because the A/D and D/A converters generate and require sampled data streams at very high sample rates, general-purpose programmable processors cannot reasonably handle these substantial DSP tasks. Instead, designers often choose ASICs targeted for the specific receive and transmit requirements of the signal channel. However, because of the variety of communication signal types and frequency characteristics, the signal processing tasks tend to be quite unique for each system. As a result, there is no single standard ASIC available to handle a wide range of applications.

Emerging Mezzanine Standards

Successful mezzanine adoption springs directly from standardization of mezzanine architectures. Standards create win-win situations by assuring customers of multiple vendor availability and competitive prices, and assuring vendors of a viable marketplace worthy of investing in product development. Several popular mezzanine standards emerging in the last few years have hit homeruns. Topping the list is the ubiquitous PMC and its unfolding series of performance enhancements.

A new standard that defines gigabit serial links to mezzanine boards for embedded communication systems is defined in the VITA 42 standard, also known as XMC[1]. As an extension to PMC, the XMC specification defines two new connectors that join the mezzanine board to the host or carrier board. At serial bit rates of 3.125 GHz, a dual connector XMC interface supports data rates of 5 Gbytes/sec in each direction.

VITA Std	Description	Type	J15 Only		J15 and J16	
			Lanes x Clock	Transfer Rate	Lanes x Clock	Transfer Rate
42.0	Base XMC Spec	-	-	-	-	-
42.1	Parallel RapidIO	Par	8 x 500 MHz	1 GB/sec	16 x 500 MHz	2.0 GB/sec
42.2	Serial RapidIO	Ser	8 x 3.125 GHz	2.5 GB/sec	16 x 3.125 GHz	5.0 GB/sec
42.3	PCI Express	Ser	8 x 2.5 GHz	2.0 GB/sec	16 x 2.5 GHz	4.0 GB/sec
42.4	HyperTransport	Par	8 x 800 MHz	1.6 GB/sec	16 x 800 MHz	3.2 GB/sec
42.5	Aurora	Ser	8 x 3.125 GHz	2.5 GB/sec	16 x 3.125 GHz	5.0 GB/sec
42.10	General Purpose I/O	-	-	-	-	-

Figure 2. VITA 42 XMC Specifications Define Specific Implementations for Popular Fabrics

Although not yet fully adopted, various draft sub-specifications for VITA 42 shown in Figure 2, define the implementation of industry standard switched fabrics. Popular serial fabric clock rates, the number of data lines, and the resulting transfer rates in each direction are shown for either one (J15) or two (J15 and J16) XMC connectors.

FPGAs in Comm Mezzanines

Among the first products to take advantage of FPGA technology are mezzanine boards. Because of this, as the features and densities of new FPGA families emerged, they significantly impacted the architectures of communication systems in many different ways. Not only can FPGAs be configured to implement numerous electrical interface standards, they can also implement a variety of communication algorithms such as modulation and demodulation, encoding and decoding, encryption and decryption, and protocol handling.

The offloading of these real-time DSP, logic and bit-rate processing tasks from general-purpose DSP or RISC processors, results in fewer processor boards in the system, and produces significant cost savings. Further, these front-end FPGA engines can extract signal information before it leaves the mezzanine module, thereby resulting in less downstream traffic and lower system data rates.

Since FPGAs can be reconfigured to perform new functions without redesigning the mezzanine board, they can accommodate new communications standards and protocols to help safeguard against product obsolescence, both at the board level and at the deployed system level. When upgrading older communication systems, a single FPGA-based product can replace several legacy products, thanks to improved logic density and flexible interfaces.

As if these benefits were not enough, FPGAs are the primary enabling technology for the new XMC gigabit serial extensions to PMC modules. During the last few years, FPGAs emerged from Xilinx featuring gigabit transceivers called RocketIO MGTs (Multi-Gigabit Transceivers), while Altera offers counterparts dubbed Stratix-GX MGTs. Data channel encoders and decoders support these physical interface drivers and include serial/parallel conversion; this way, data and clock are combined in the signaling on each differential pair over the external serial channel. SERDES (SERializer/DESerializer) blocks built right into the FPGA, include circuitry for both the receive and transmit functions.

A protocol engine within the FPGA interfaces with the SERDES to correctly process packets, header information, control functions, error detection and correction, and payload data format. Since each switched serial fabric standard has its own protocols and rules, FPGAs offer unmatched flexibility by allowing users to install the appropriate IP core protocol engine. The strategy makes FPGA-based XMC modules truly "fabric agnostic" and allows one hardware design to be deployed in several different fabric environments. ➤

[1] More information on XMC was presented in the Spring 2007 Pipeline issue

Mezzanine Board Strategies for Communication Systems

Enhanced Digital Downconverter

By taking advantage of FPGA technology to extend the bandwidth range of the ASIC devices, commercial off-the-shelf mezzanine modules for communication systems can become flexible enough to satisfy a wider range of markets and signal types.

Figure 3 shows a typical software radio transceiver PMC/XMC mezzanine module for communication systems. It features two 14-bit 105 MHz A/Ds and two 16-bit 500 MHz D/As connected to a Xilinx XC2VP50 FPGA. Two ASIC devices handle DDC and DUC functions with memory, timing and system interfaces completing the product. Note that the XMC interface uses the built-in RocketIO gigabit serial transceivers of the FPGA.

The DDC ASIC is a Texas Instruments GC4016 four-channel narrowband device with decimation settings ranging from 32 to 16,384. Since channel bandwidth is inversely proportional to the decimation factor, a factor of 32 limits the maximum usable channel bandwidth to 2.5 MHz[2], falling far short of many communication signal types.

To handle wider signals, two wideband DDC IP cores, installed in the FPGA, with decimation settings ranging from 2 to 64, deliver a maximum channel bandwidth of 40 MHz for both A/Ds. Programmable data switches inside the FPGA allow the wideband DDC cores to be driven directly from the A/D converter or in cascade from the outputs of the GC4016 DDC. This extends the maximum decimation of the GC4016 by a factor of 64. By including the new wideband DDC core, the overall decimation range for the mezzanine now becomes 2 to 1,048,576 instead of the previous 32 to 16,384. This extended range translates directly to an enormous range of input signal bandwidths from 76 Hz to 40 MHz.

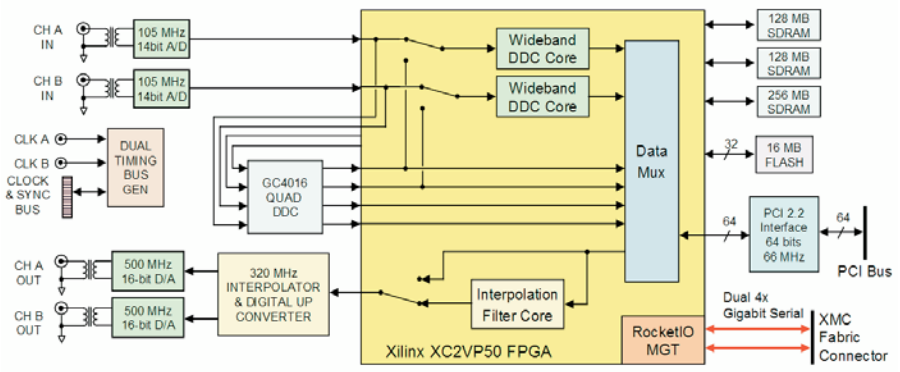


Figure 3. Model 7140-420 Software Radio Transceiver XMC mezzanine with Communication IP Cores

Enhanced Digital Upconverter

The DUC ASIC is a Texas Instruments DAC5686 wideband device with interpolation settings of 2 to 16. Like the DDC, the output channel bandwidth is inversely proportional to the interpolation factor, so with a maximum interpolation setting of only 16, narrowband transmit signals are not supported. To handle narrowband signals, an interpolation filter is installed in the FPGA with programmable interpolation factors from 16 to 1024. Again, a programmable data switch allows the ASIC DUC to be driven directly from the data interface for wideband signals or from the output of the interpolation filter for narrowband signals. With the interpolation core, the overall interpolation range extends from 2 to 16,384 instead of the previous 2 to 16. Output signal bandwidths from 4.8 kHz to 40 MHz can now be accommodated.

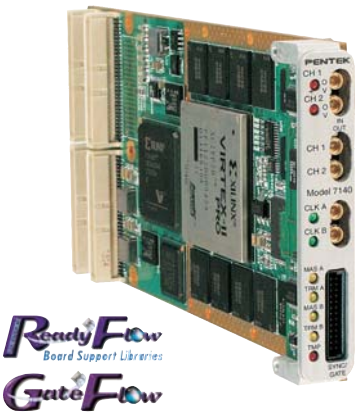
Since all of these critical functions fit in the compact PMC form factor shown in Figure 4, it's easy to see why FPGAs have been so widely deployed on mezzanine modules for communication systems. Of course, many other signal processing tasks, such as those shown in the transmit and receive signal processing blocks in Figure 1, can also be handled by the FPGA.

Beamforming Techniques

More sophisticated signal processing operations, such as beamforming, can lead to significant improvements in communication systems. Examples abound along the highway where numerous cellphone towers with vertical antenna arrays, usually in groups of four, can be seen. Signals from multiple receive antennas can be phase-shifted by using the mezzanine module memories as digital delay blocks to enhance reception of a signal arriving from a specific direction. Likewise, transmission using multiple antennas with phase-shifted signals can steer the outgoing signal towards a specific target. This not only provides better service to subscribers but also allows frequency reuse within a cell by dividing the cell into beamformed sectors.

A Secure Future for Mezzanines

Mezzanines will continue to play important roles in communication systems; they offer an excellent solution to local high-performance signal acquisition and preprocessing, saving costly processor resources in the rest of the system. With FPGAs on board, mezzanines can be reconfigured to meet new communications standards extending the life cycle of existing systems. When new critical ASIC devices emerge, the standardization and modularity of mezzanines supports new technology insertion by simple replacement, rather than scrapping a whole system. This modularity also reduces maintenance, troubleshooting and service costs. Finally, the switched fabric interfaces already available in many mezzanine modules ensure plenty of data bandwidth for future wideband signals. ❑



For more information on the 7140 click here: pentek.com/go/pipe7140

Figure 4. Model 7140 PMC/XMC Module

[2] For sampling frequency of 100 MHz and 80% filter

Product Focus
Model 6890

Clock, Sync and Gate Distribution VME Board

With up to 2.2 GHz clock, the new Model 6890 supports the Model 6826 A/D Converter Board

General Information

Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Features

- Synchronizes up to eight separate boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates from 800 MHz to 2.2 GHz
- Front panel SMA connectors for clock input and outputs
- Front panel MMCX connectors for gate/trigger and sync signal inputs and outputs
- Single-slot 6U VME board

Model 6890 (left) shown with the Model 6826 2.0 GHz A/D Converter

Input Signals

Model 6890 provides three front panel connectors to accept input signals. One SMA connector is provided for clock signal input, one MMCX connector accepts gate or trigger signals, and another MMCX connector is provided for synchronization. Two additional MMCX connectors are provided for Gate and Sync Enable.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

Clock Signals

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors.

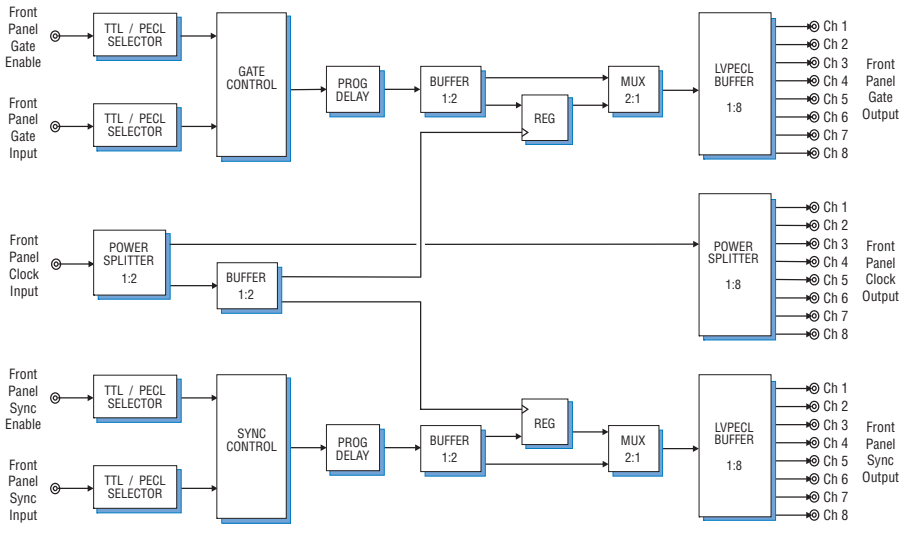
The second output of the 1:2 power splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

Gate and Synchronization Signals

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable MMCX inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.



Accessories

Model 2890 provides various cable sets with options -002 through -008 supporting synchronization of two to eight boards. Options for individual cables are also available under Model 2890.

Supported Products

The 6890 currently supports the Model 6826 Dual 2 GHz, 10-bit A/D Converter VME Board. Contact the factory for an up-to-date list of supported boards and modules.

For more information and a price quotation on the Model 6890, click here:
pentek.com/go/pipe6890

For more information and a price quotation on the Model 6826, click here:
pentek.com/go/pipe6826 ❑

Product Focus

Model 7140-420

GateFlow Transceiver with Dual Wideband DDC and Interpolation Filter - PMC/XMC

7140-420 Installed Core

General Information

Model 7140-420, Dual Digital Transceiver with Wideband DDC and Interpolation Filter cores, is a complete software radio system in PMC/XMC format. It includes two A/D and two D/A converters for connecting to HF or IF ports of a communications or radar system.

The 7140 receiver section features two AD6645 105 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, Pentek offers the GateFlow IP Core 420 High-Performance Wideband DDC and an interpolation filter that extends the range of the DAC5686 D/A converter.

ReadyFlow Board Support Libraries GateFlow

Features

- Complete software radio transceiver solution
- GateFlow Core 420 dual high-performance wideband DDCs and interpolation filter factory-installed
- Improved dynamic range
- Extended DDC decimation range of 8 to 1,048,576
- Extended DDC bandwidth range of 10 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 16,384
- Extended DUC bandwidth range of 40 MHz to 4.88 kHz

Core 420 Wideband DDC

The Core 420 downconverter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

Two identical Core 420 DDCs are factory installed in the 7140 FPGA. The decimation range from 2 to 64 in six binary steps provides output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

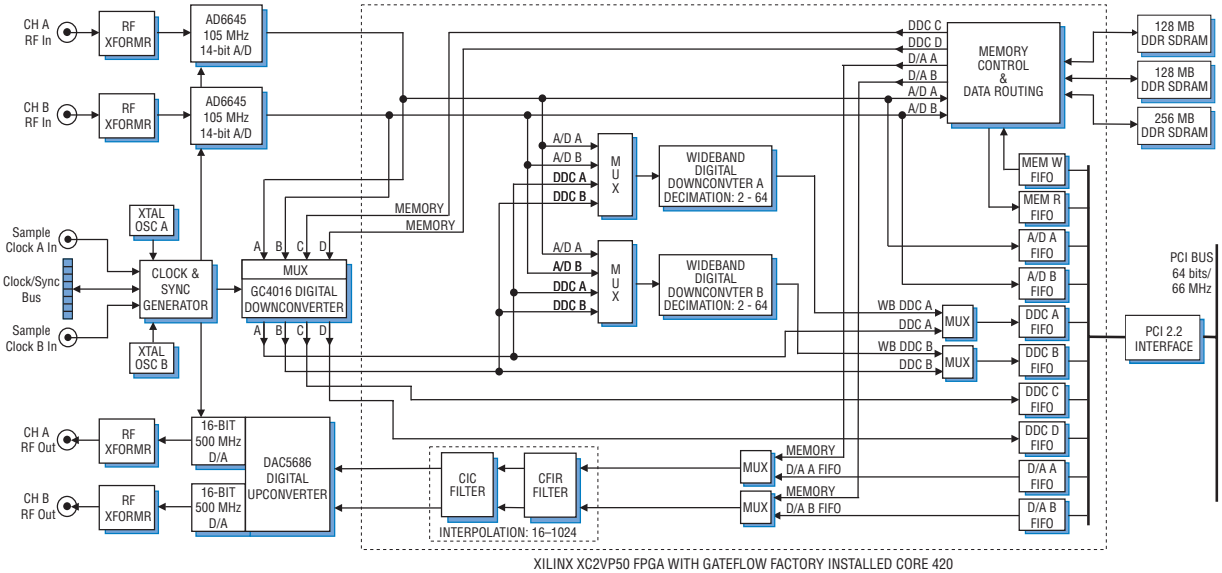
The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 16,384 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 16,384 which matches the maximum decimation of the GC4016 narrowband DDC.

Core 420 is also available for cPCI Models 7240, 7340 and PCI Model 7640.

Conduction-cooled version is availalable with Model 7141-703.

For more information and a price quotation on the 7140-420, click here:

pentek.com/go/pipe7140-420 ❑



XILINX XC2VP50 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 420