Georgia Tech Develops an Adaptive System for Satellite Communications

Starting in the mid-1990's, Low-Earth-Orbiting (LEO) satellites were deployed to provide full global voice and data communication services. While less expensive to launch than Geosynchronous (GEO) satellites that provide the familiar DIRECTV and DISH Network television services, the LEOs require large 10-meter ground dish antennas that have to be steered through as much as 160 degrees. To maximize contact with the polar orbiting satellites, the ground stations are near the poles and they are very expensive to build and maintain.

Researchers at the Georgia Institute of Technology in collaboration with NASA's Glenn Research Center and the University of Colorado have been investigating the feasibility of a remotely programmable ground station with ideally no moving parts, in non-polar regions, and a cost objective of less than one-tenth the cost of a present ground station to build and maintain.

Rather than utilizing a single large dish, the ground system would use a number of phased antenna arrays with their outputs adaptively combined to maximize the signal-to-interference-and-noise ratio of the desired satellite transmission. The vision of the Georgia Tech researchers is that these ground stations would be connected via the internet, so that any LEO satellite can be in practically continuous communication with the Earth network. The focus of their project is the design of the RF front end and digital signal processing of the phased array outputs.

Adaptive Signal Processing

The adaptive combination of the signals from multiple antennas provides several features: array gain, interference suppression, diversity gain, and multiple user detection. Array gain is entirely a

Figure 1. Four Helical Antennas Receiving the Signal from EO-1 (Courtesy of Georgia Tech)

function of the number of antenna elements. Interference suppression occurs when the adaptive array creates a null in the direction of the interference. Diversity gain is the difference in the depths of individual antenna element signal fades such as those caused by multipath reflections, and the depth of fades in the output of the adaptive combiner. Finally, multi-user detection allows multiple interfering signals to be separated by the adaptive combiner.

Two additional signal processing functions are necessary in the adaptive combiner, frequency synchronization and steering of the directional elements (DE) of the antenna array to keep the DEs pointed in the direction of the satellite.

In the first year of this project, a prototype system was built to demonstrate adaptive signal processing. Four DEs were utilized for the 4 kb/sec downlink of the EO-1 satellite. Synchronization, array gain,

and diversity gain were demonstrated. The DEs were fixed and not scanned, so DE steering was not necessary.

Prototype Front End

Four homemade helical antennas were used on the roof of the 5-story GCATT (Georgia Centers for Advanced Telecommunication Technology) building as shown in the photo of Figure 1. Each antenna has a 3 dB bandwidth of approximately 45°, right-hand circular polarization and a gain of around 11.4 dB at 2.27 GHz (S-Band).

The urban environment in Atlanta, GA presents certain challenges to the design of the RF front end. The problems encountered are PCS cellular phones and satellite radio. While PCS is located more than 250 MHz away from the EO-1 satellite signal, XM and Sirious radio signals are as close as 50 MHz to EO-1 and more than 60 dB stronger! ➤

Georgia Tech Develops an Adaptive System for Satellite Communications

[Continued from page 1]

These interfering signals can reduce the sensitivity of the RF front end and can also cause severe intermodulation distortion.

To reduce these interference problems, a very narrowband and low-loss bandpass filter was developed. Two low noise amplifiers (LNAs) were used, one following the antenna and the other following the bandpass filter. The final analog output was then applied to the APCOM analog downconverter. Its output is a 16 MHz IF suitable for A/D conversion by the Pentek 6235 2-channel A/D Converter VIM-2 module.

Figure 2. Data Acquisition System Block Diagram

Data Acquisition System

The complete data acquisition system is shown in Figure 2. The outputs of the four helical antennas are amplified by the four commercial LNAs which are followed by the custom-developed bandpass filters. Another set of LNAs provides additional gain and feeds the signal into the APCOM analog downconverters. In turn, their outputs are fed to two Pentek Model 6235 dual wideband digital receivers with 12-bit 65 MHz A/Ds VIM-2 modules, which sample the 16 MHz IFs.

The digital downconverters of the Model 6235 convert these to complex baseband. Each 6235 is mounted on a Pentek Model 4291 quad C6701 floating-point DSP processor board which is used to control data acquisition and signal routing. Pentek Model 6226 FPDP adapter VIM-2 modules are also mounted on these two processor boards to transfer the data to two workstations for data storage and post processing calculations.

Frequency Synchronization

Because of the motion of the satellite, Doppler shifts cause the center frequency to change by as much as 1 kHz per second. To improve tracking, a phase lock loop was implemented in post processing to follow the carrier frequency of the satellite. Frequency synchronization was performed separately for each antenna. This was found to yield better results than performing synchronization for one antenna and then applying the correction to all.
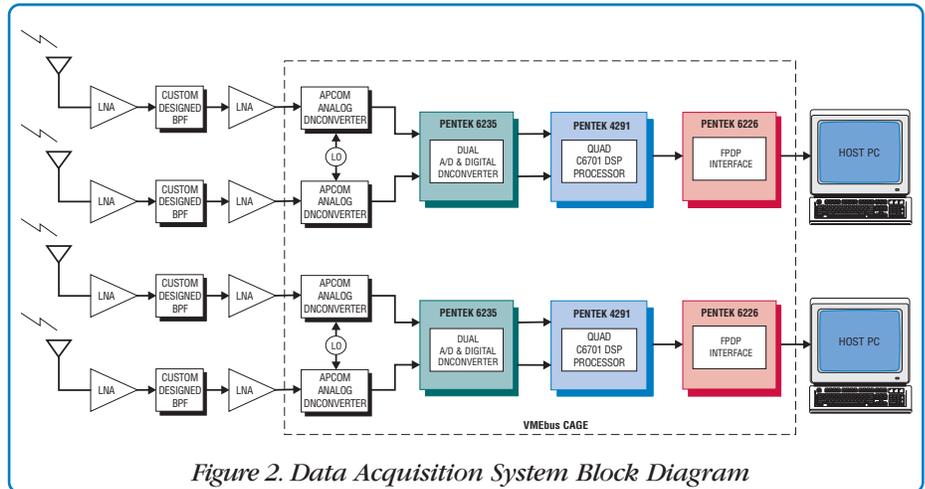
The Adaptive Combiner

The outputs of the phase locked loops are adaptively weighted and summed. An error signal is formed by subtracting the output of the combiner from the ideal version of the signal based on a training signal. The adaptive algorithm iteratively adjusts the weights to drive the error to zero. When the average power of the error is minimized, the algorithm is considered to have converged.

Results

Experimental results were measured during a satellite pass on April 7, 2004. The average SNR of the adaptive combiner was 27.3 dB. To demonstrate diversity gain, a second pass was conducted on April 30, 2004. This time, instead of having the four helical antennas out in the open, they were enclosed in a 30 ft x 30 ft walled area without a ceiling on top of the GCATT building. This arrangement was made to create multipath by having the satellite signals reflect from the walls. The antennas were spaced 6–8 ft apart. The results are shown in Figure 3. The lower four curves are the individual results from the four antennas; their fluctuation indicates multipath fading. The curve at the top is the combiner output and it clearly shows the diversity gain effect.

Future Plans

In the follow up investigations, a X-band system will be constructed. It will receive its signals from the SAC-C satellite which travels in the same constellation as the EO-1. The new satellite has a data rate of 6 Mb/sec and a bandwidth of 24 MHz which is the maximum that can be accommodated by the present data acquisition system. In addition, the DEs will be steered.

The DEs may be small dish antennas, or phased antenna arrays presently being developed at the Glenn Research Center and the University of Colorado. One of these is a "space-fed lens" array, while the other is a "reflectarray" containing integrated phase shifters and patch radiators. Either one of these can be used as the directional element of the adaptive combiner. The result will be a ground station that provides extreme flexibility in connecting low-earth-orbiting satellites with the Earth network without moving parts and costing a fraction of the cost of today's ground stations. ❏
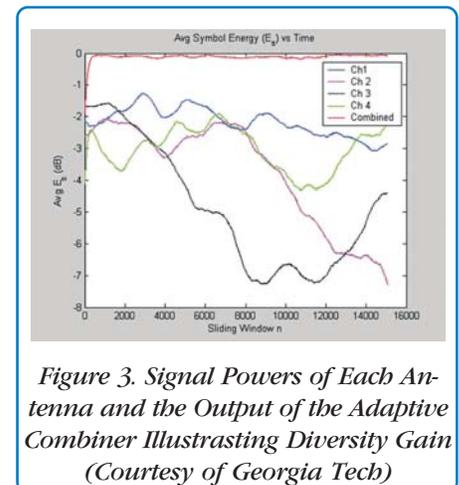

Figure 3. Signal Powers of Each Antenna and the Output of the Adaptive Combiner Illustrating Diversity Gain (Courtesy of Georgia Tech)

Comprehensive Software Radio Transceiver PMC/XMC Module

[From page 4]

status engine with data and programming interfaces to each of the on-board resources. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

Because the FPGA controls the data flow within the module as well as providing signal processing, the module can be configured for many different functions. In addition to acting as a simple transceiver, the module can perform user-defined DSP functions on the baseband signals, developed using Pentek's GateFlow and ReadyFlow development tools.
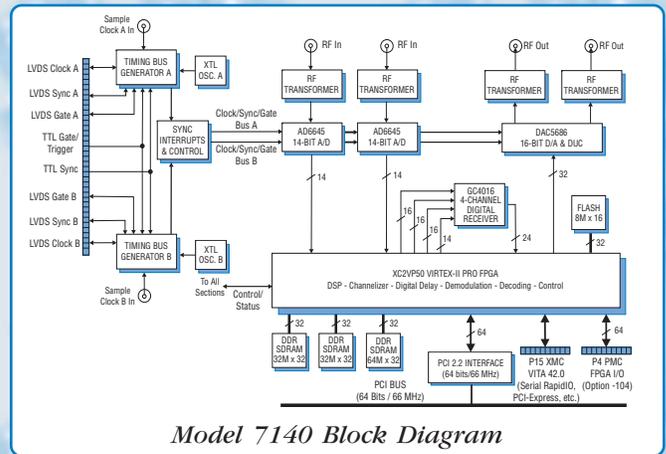
Digital Up/Downconverters

The module includes a TI/Graychip GC4016 quad digital downconverter along with a TI DAC5686 digital upconverter with dual D/A converters. Each channel in the downconverter can be set with an independent tuning frequency

and bandwidth. The upconverter translates a real or complex baseband signals to any IF frequency from DC to 160 MHz and can deliver real or complex (I+Q) analog outputs through its two 16-bit D/As. The upconverter can be bypassed for two interpolated D/A outputs with sampling rates to 500 MSPS.

Synchronization Capabilities

A clock/sync bus allows synchronization of local oscillator phase, frequency switching, decimating filter phase and data collection among multiple 7140s. One board acts as a master, driving clock, sync and gate signals out to a

Model 7140 Block Diagram

front panel flat cable bus using LVDS differential signaling. The master alone can drive as many as seven slaves. By using a Pentek Model 9190 Clock and Sync Generator to drive the signals, as many as 80 modules can be configured to operate synchronously. For more information on the Model 7140 Transceiver visit www.pentek.com/go/pipe7140. ❏

New Development System Platform and SystemFlow™ Software

New!

The new Pentek Model RTS 2503 is a scalable real-time platform for data acquisition, processing, analysis and recording of wideband signals to 215 MHz sampling. Including the latest A/Ds, FPGAs and PowerPC processors, the platform allows you to take advantage of the latest technology for signal processing.

Scalable from 1 to 20 channels in a single 6U VMEbus enclosure, the RTS 2503 serves equally well as a development platform and proof-of-concept prototype—or as a cost effective approach to deploying high-performance multi-channel embedded systems.

The heart of the RTS 2503 is the Pentek Model 4205 I/O processor board

featuring a 1 GHz MPC7457 PowerPC with mezzanine sites for both PMC and VIM modules. The board includes two Xilinx Virtex-II FPGAs which are supported by Pentek's GateFlow™ FPGA Resources. GateFlow includes the FPGA Design Kit, FPGA IP Core Libraries and FPGA factory-installed cores for out-of-the-box performance without the need for FPGA code development.
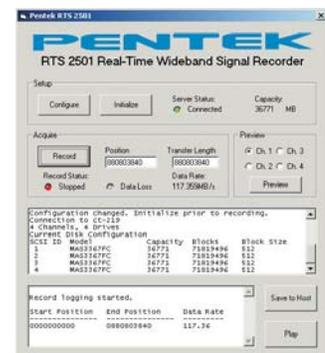
Built-in Fibre Channel and optional RACE++ and Gigabit Ethernet interfaces provide excellent I/O connectivity without sacrificing any of the mezzanine sites. For more information, visit www.pentek.com/go/piperts2503.

The Model 4990 SystemFlow API (Application Programming Interface) and Development Libraries provide a rich set of tools and function libraries for building data acquisition and recording systems based on the Pentek RTS Real-Time Development Platforms.

A prebuilt turnkey wideband signal recorder system example is included. Its GUI (Graphical User Interface) provides

an easy-to-use control panel for recording and playback of wideband data. In addition to providing a basic recording system, this application is an excellent base for custom system development.

SystemFlow consists of a Windows host application running on an Intel based PC and an eCos target application running on the Pentek 4205 PowerPC I/O processor board that's included in the RTS Development Platform. For more information, visit www.pentek.com/go/pipe4990. ❏

Model 4990 Record Control Interface

Please visit pentek.com/delivery to enter your delivery preferences for new product information.

3

Product Focus

Model 7140

GateFlow
ReadyFlow
Board Support Libraries

This PMC/XMC board is also available in conduction-cooled, cPCI and PCI formats.

Comprehensive Software Radio Transceiver Packs FPGA Processing Power with XMC Switched Fabric I/O

Features

- Dual digital upconverter/downconverter handles 40 MHz bandwidth RF or IF signals
- Xilinx Virtex-II Pro FPGA with two PowerPC cores for application engines
- Configurable data routing puts FPGA processing in the baseband data stream
- XMC I/O for high-speed data streaming with switched backplane fabrics
- Dual timing buses for independent input and output clocks
- LVDS clock/sync bus for multiple module synchronization
- 512 MB memory to buffer data for digital delay or data capture
- Compatible with Pentek GateFlow® IP Cores and FPGA Design Tools
- Pentek ReadyFlow® Board Support Libraries for quick board setup
- Ideal for SIGINT and JTRS applications

The Model 7140 PMC module combines both transmit and receive capability with a high-performance Virtex II-Pro FPGA and supports the emerging VITA 42 XMC standard with optional switched fabric interfaces for high-speed I/O. This module is also available in a variety of form factors including PCI (Model 7640), 3U cPCI (Model 7340), 6U cPCI (Model 7240) and a PMC/XMC conduction-cooled version (Model 7140-700).

The front end accepts two +4 dBm full-scale analog RF inputs and transformer-couples them into two 14-bit A/Ds sampling at up to 105 MHz. The digitized output signals pass to a Virtex-II Pro FPGA for signal processing or routing to other module resources. These include a quad digital downconverter, a digital upconverter with dual D/As, 512 MB DDR SDRAM delay memory and the PCI bus. The FPGA also serves as a control and ▶