Models 7241, 7241D and 7341 with Core 420

GateFlow Transceiver with Dual/Quad Wideband DDCs and Interpolation Filters - 3U/6U cPCI

Model 7341-420

Model 7241D-420

ReadyFlow Board Support Package

GateFlow

Features

- GateFlow Core 420, two high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 2 to 1,048,576
- Extended DDC bandwidth range of 40 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 32,768
- Extended DUC bandwidth range of 40 MHz to 2.44 kHz

General Information

Models 7241-420 and 7341-420 are cPCI Transceivers with Dual Wideband DDCs and Interpolation Filters. They consist of one Model 7141-420 transceiver mounted on a cPCI carrier board. Model 7241-420 is a 6U cPCI board, while the Model 7341-420 is a 3U cPCI board. Model 7241D-420 is the same as the Model 7241-420, except it contains two 7141-420's rather than one.

The receiver section features two or four LTC2255 125 MHz 14-bit A/D converters and one or two TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, these boards include Pentek's GateFlow Installed Core 420 high-performance wideband DDC, similar in functionality to the GC1012 but with enhanced performance, and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 downconverter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

Two identical Core 420 DDCs are factory installed in the FPGA. The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

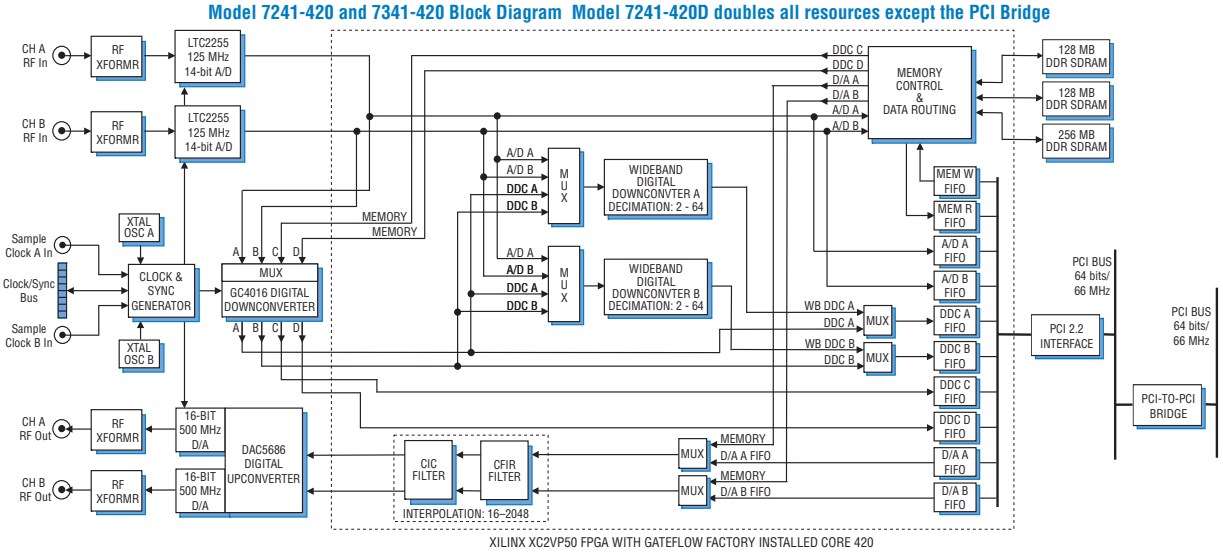
A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of these Models are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤

Model 7241-420 and 7341-420 Block Diagram Model 7241-420D doubles all resources except the PCI Bridge



XILINX XC2VP50 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 420

PENTEK

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GateFlow Transceiver with Dual/Quad Wideband DDCs and Interpolation Filters - 3U/6U cPCI

Ordering Information

Model	Description
7241-420	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - 6U cPCI
7241D-420	GateFlow Transceiver with four Wideband DDCs and two Interpolation Filters factory-installed - 6U cPCI
7341	GateFlow Transceiver with two Wideband DDCs and Interpolation Filter factory-installed - 3U cPCI

Contact Pentek for available options

➤ Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to four slave 7241D-420's or seven 7241-420's or 7341-420's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to eighty 7241-420 or 7341-420 boards, or forty 7241D-420 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to each FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Interface

An industry-standard interface fully compliant with PCI 2.2 bus specifications is included. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

7241-420: Dual Configuration; 7241D-420: Quad Configuration; 7341-420: Dual Configuration
7241D-420 shown in the Specifications
Analog Signal Inputs (4)
Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB
Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz
A/D Converters (4)
Type: Linear Technology LTC2255
Sampling Rate: 1 MHz to 125 MHz
Internal Clock: Crystal oscillator A or B
External Clock: 1 to 125 MHz
Resolution: 14 bits
Digital Downconverters (2)
Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data
Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096
Front Panel Analog Signal Outputs (4)
Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz
Digital Upconverters (2)
Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits
Clock Sources (4): Selectable from onboard A or B crystal oscillators, external or LVDS clocks
External Clocks (4)
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
Sync/Gate Bus (2): 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal
Field Programmable Gate Array (2)
Type: Xilinx Virtex-II Pro XC2VP50
Memory
DDR SDRAM: 1 GB in six banks
FLASH: 32 MB in two banks.
PCI Interface
PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
Local Bus: 64-bit, 66 MHz
DMA: 9 channel demand-mode and chaining controller
Environmental (Commercial version)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Size: Standard 6U cPCI board

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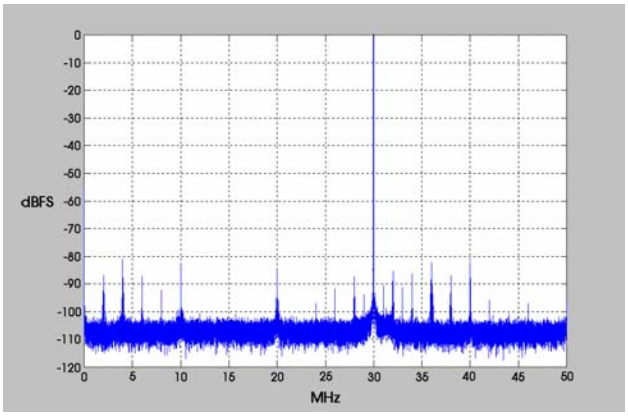
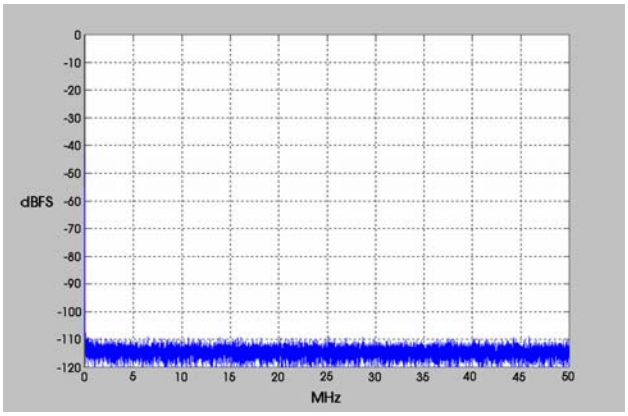
A/D Performance

Spurious Free Dynamic Range



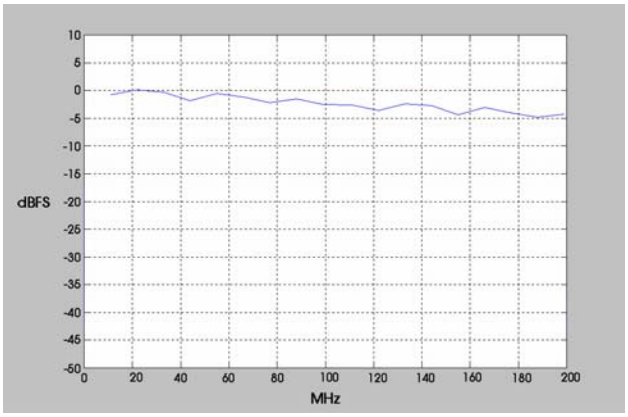
f_{in} = 70 MHz, f_s = 100 MHz

Spurious Pick-up



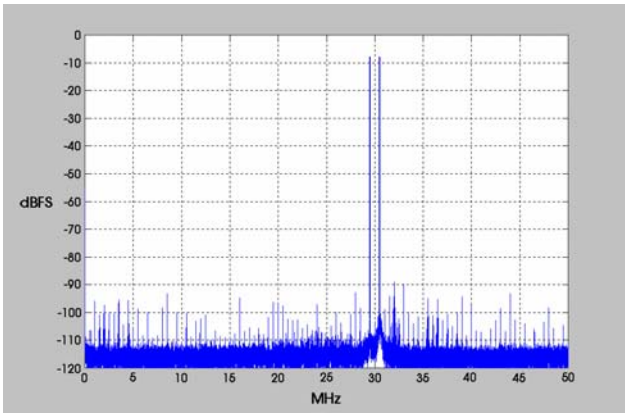
f_s = 100 MHz, 32k point FFT, 8 averages

Input Frequency Response



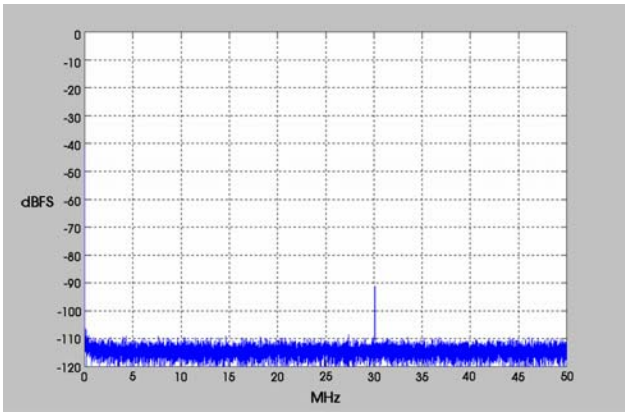
f_s = 100 MHz

Two-Tone SFDR



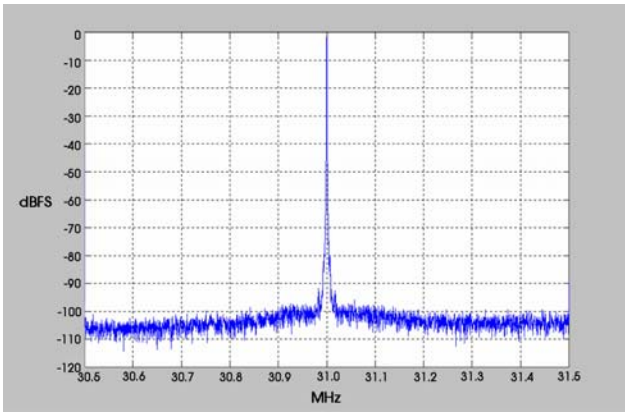
f_1 = 29.5 MHz, f_2 = 30.5 MHz, f_s = 100 MHz

Crosstalk



$f_{in\ Ch2}$ = 69 MHz, f_s = 100 MHz, Ch 1 shown

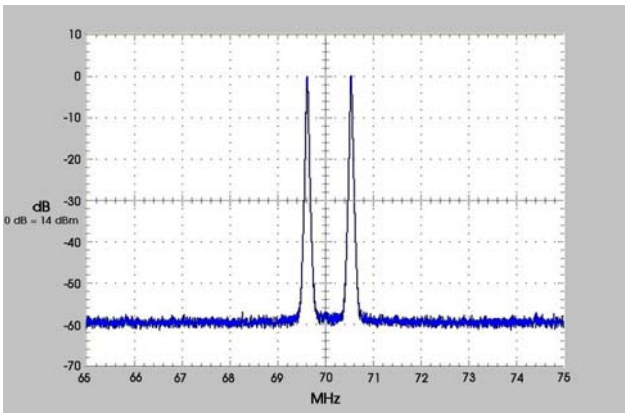
Phase Noise



f_{in} = 69 MHz, f_s = 100 MHz
Phase Noise @ 100 kHz = -102 - 10*log(610) = -129.8 dB/Hz

D/A Performance

Two-Tone Intermodulation Distortion



f_1 = 69.5 MHz, f_2 = 70.5 MHz, f_s = 100 MHz