Model 6821-422 Installed Core

GateFlow 215 MHz A/D and Digital Receiver - VME

Model 6821-422 commercial (left) and conduction-cooled version.

ReadyFlow Board Support Package

GateFlow

Features

- AD9430 12-bit 215 MHz A/D converter
- Dual GateFlow Core 422 296 MHz wideband DDCs, factory-installed
- Four sets of 18-bit user-programmable FIR filter coefficients
- Four FPDP or FPDP II front panel outputs
- FIFO buffering for real-time recording
- Xilinx Virtex-II Pro FPGAs
- ***Ruggedized and conduction-cooled versions available***

General Information

Model 6821-422 GateFlow 215 MHz A/D and Digital Receiver is a high-frequency single channel A/D converter with built-in digital downconverters. It accepts one front panel analog input and delivers digital output samples over two or four FPDP connectors utilizing FPDP or FPDP II standards. LVDS I/O is also available.

The 6821 features an Analog Devices AD9430 12-bit A/D converter with a maximum sampling rate of 215 MHz. To convert this board into a complete software radio system, Pentek has added the GateFlow IP Core 422 High-Performance Wideband DDC similar in functionality to the Texas Instruments GC1012B, but with enhanced speed, performance and programmability.

In standard 6821 units, the Virtex-II Pro FPGAs contain factory-programmed code to implement control, initialization, mode selection and data formatting functions. Since most of the FPGAs remain available for custom algorithms, Pentek offers the 6821-422 as a factory installation of two complete channels of the GateFlow IP Core 422 (one channel per FPGA).

Architecture

The block diagram below shows the AD9430 A/D converter driving the Core 422 Wideband DDC, and also bypassing the DDC core for a direct connection to the output FIFOs.

The 6821-422 features up to four FPDP connectors for data output. Several data packing modes are selectable across the multiple FPDP ports.

Alternatively, LVDS I/O is available through either the VMEbus P2 connector or a second-slot front panel mezzanine.

Core 422 Digital Downconverter

The Core 422 DDC translates any frequency band within the input bandwidth range down to zero frequency, performs low pass filtering, and then combines and decimates the filter output for delivery as real or complex samples.

Pairs of consecutive even and odd input samples from the A/D are delivered to the core at half the sample clock frequency. An input gain stage allows scaling of the A/D data samples by a 16-bit gain term.

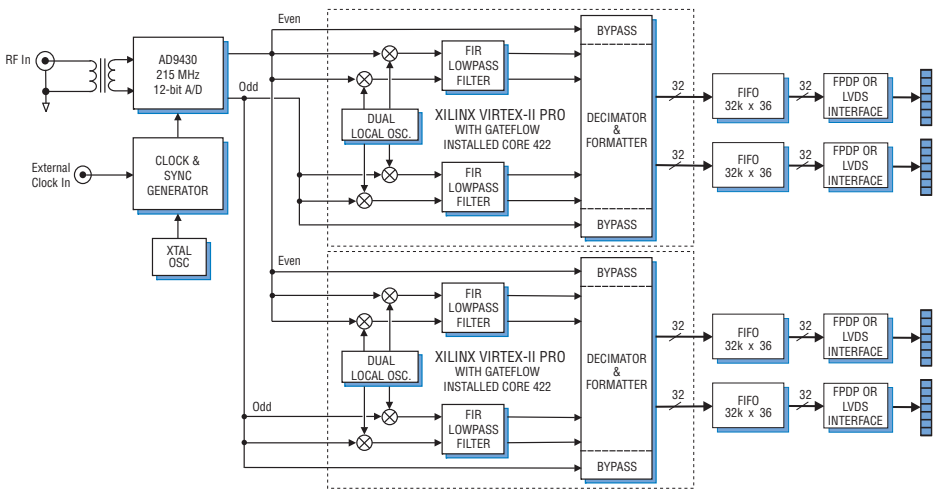
A dual complex NCO delivers pairs of even and odd complex local oscillator samples to four 18x18 multipliers which implement the complex mixer. The programmable NCO provides over 110 dB spurious-free dynamic range (SFDR).

The dual FIR low pass filter can store and utilize up to four independent sets of 18-bit coefficients for each of six decimation settings: 2, 4, 8, 16, 32 and 64. Two default coefficient sets for 80% and 90% passband filters are also available:

Default Filter	Usable Bandwidth	Passband Ripple	Stopband Rejection
80%	0.8 Fs	< 0.08 dB	> 100 dB
90%	0.9 Fs	< 0.50 dB	> 75 dB

Fs = Complex Output Sample Rate

A DDC bypass path allows the A/D input data to be sent directly to the output formatting stage for delivery to the FPDP or LVDS outputs for data acquisition applications that require no downconversion. ➤



➤ Clocking, Gating and Triggering

The A/D converter sample clock can be sourced from an internal 210 MHz crystal oscillator or from an externally supplied sinusoidal clock of 215 MHz, maximum. This clock is accepted through a front panel SMA connector terminated in 50 ohms.

An external LVDS bus supports synchronous data acquisition across multiple boards. This is ideal for applications such as multichannel radar systems.

FIFOs and FPDP Outputs

Following each FPGA are two 32-bit wide FIFO buffers with standard depth of 32k words. These FIFOs are useful as elastic memory to support hard disk latencies in recording applications.

A total of four FPDP output ports are available, two per FPGA, to support data transfers of 320 MB/sec each or greater. One port per FPGA is attached to the board's front panel, with the second attached to an optional second-slot front panel.

A data demultiplexing mode splits the data stream between each pair of FPDP ports, reducing the output data rate by a factor of up to four (depending on the data packing mode and number of FPDP ports) to support slower FPDP devices.

VXS Interface

Model 6821-422 provides optional full duplex VITA-41 VXS links to the VME P0 connector for both FPGAs. These links support 4X Serial RapidIO, or other switched fabrics such as PCI Express and Xilinx Aurora.

Specifications

Front Panel Analog Signal Input
- **Input Type:** Transformer-coupled, front panel female SMA connector
- **Full Scale Input:** +8 dBm (1.59 V p-p) or + 2 dBm (0.796 V p-p), software selectable, into 50 ohms
- **Input Bandwidth:** 150 MHz
- **Transformer 3 dB Passband:** 400 kHz to 700 MHz

A/D Converter
- **Type:** Analog Devices AD9430-210
- **Sampling Rate:** 60 MHz to 215 MHz
- **Internal Clock:** 210 MHz crystal oscillator
- **External Clock:** 60 to 215 MHz
- **Resolution:** 12 bits
- **Bandwidth:** 700 MHz at full power

Clock Source: Onboard crystal oscillator, front panel external clock

External Clock: Front panel female SMA connector, sine wave, 0 to +4 dBm, AC coupled, 50 ohms impedance

Sync/Gate Bus: One 26-pin connector with one clock, one FPGA sync, and four gate input/output LVDS signals; one sync and one gate input TTL signals

Field Programmable Gate Arrays
Two Virtex-II Pro XC2VP50-5

Front Panel Data Port (FPDP) Outputs
- **Quantity:** 2 standard
- **Output Type:** non-inverted configuration, FPDP I or FPDP II
- **Clock:** Onboard programmable oscillator (up to 50 MHz), or sample clock with one line to each FPDP port

FIFOs
- **Quantity:** 2 standard
- **Size:** 32,768 x 36
- **Speed:** Sample clock rate ÷ 2

VME Slave Interface
- **Type:** Slave A16/D16, A16/D32 (A32/D32 programmable)
- **Control:** Operating modes, gate/trigger, FIFO reset, data packing, FPDP I/II selection, FPDP framing, time sync command, status

Power
62 W maximum

Environmental (Commercial version)
- **Pentek Ruggedization Level:** L0
- **Cooling Method:** Forced air
- **Operating Temp:** 0 to 50° C
- **Storage Temp:** –20 to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing

Environmental - Option -703
- **Pentek Ruggedization Level:** L3
- **Cooling Method:** Conduction cooling
- **Operating Temp:** –40 to 70° C
- **Storage Temp:** –50 to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing
- **Sine Vibration:** 10 g, 20–2,000 Hz
- **Random Vibration:** 0.1 g^2/Hz, 20–2,000 Hz
- **Shock:** 30 g, 11 ms

Environmental - Option -720
- **Relative Humidity:** 0 to 100% non-condensing with conformal coating

Size: Standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 20.3 mm (0.8 in) wide; Option -222 or -224: 40.6 mm (1.6 in) wide

Weight: 425 grams (15 oz.); 794 grams (28 oz.) conduction-cooled version

Ordering Information

Model	Description
6821-422	215 MHz, 12-bit A/D with Wideband 296 MHz DDC Core factory-installed - VME

Contact Pentek for available options

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