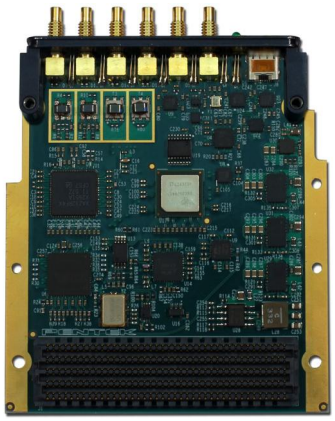
New!

Model 3320

2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A - FMC



FlexorReadyFlow Board Support PackageGateFlow

Features

- Sold as the:
  - FlexorSet Model 5973-320
  - FlexorSet Model 7070-320
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Ruggedized and conduction-cooled versions available

General Information

The Flexor™ Model 3320 is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

The 3320 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-320 3U VPX or the FlexorSet 7070-320 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

Performance of the Model 3320

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion modes. Users can use these modes which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own modes via the PCIe interface. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

A/D and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for pre-configured modes.

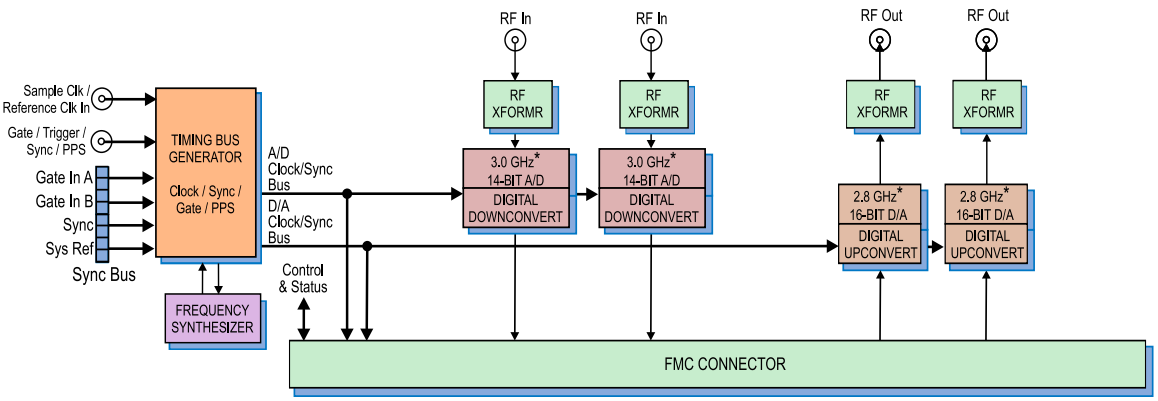
A/D Acquisition IP Modules

With the 3320 installed on either the 5973 or the 7070 carrier, the board-set features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the two D/A waveform playback IP modules in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier's PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's job of identifying and executing on the data. ➤



* See last page for configuration modes

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Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC39J84 D/As accept two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide interpolation factors from 1x to 16x.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 5973 or the 7070, the FlexorSet's built-in functions include setup and support of the timing generator to produce the predefined data conversion modes. This simplifies operation by allowing users to easily change modes through software.

The timing bus generator has a built-in frequency synthesizer that allows the board to operate without the need for an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the board can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes two gates, sync, and Sys Ref signals. Multiple 3320s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

In addition to the µSync bus, a front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync. Users can program the connector's function to operate in one of three modes to match the application requirements.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek's ReadyFlow® BSP provides control of all the 3320's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek's GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973-320 or 7070-320 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface

The Model 3320 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3320 and the FMC carrier. ➤

Ordering Information

3U VPX

Model	Description
5973-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

8267	VPX Development System See 8267 Datasheet for Options

PCIe

Model	Description
7070-320	2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - x8 PCIe
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

8266	PC Development System See 8266 Datasheet for Options

➤ Model 3320 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

A/D Converters
- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See table below

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 4x with pre-configured conversion modes, other decimations available with custom programing

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel SSMC connectors

Transformer Type: Coil Craft WBC4-14L

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See table below

Digital Upconverters
- **Quantity:** Two channels
- **Interpolation Range:** 2x and 4x with pre-configured conversion modes, other interpolations available with custom programing

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
- **Frequency Range:** 1.3 to 3.0 GHz

Sync Bus: 19-pin µSync bus connector includes two gates/triggers, a sync and Sys Ref inputs, CML

External Trigger Input
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Pre-configured Modes

The Model 3320 is delivered with a set of six pre-configured modes. These allow users to easily select A/D and D/A settings that are commonly used in many applications. While these modes typically satisfy many applications, users can always configure the A/D and D/A setting to their specific requirements via the PCIe interface using the ReadyFlow Board Support Package.

Pre-configured Conversion Modes

	A/D Converter							D/A Converter					
mode	sample rate	DDC or bypass	output bits resolution	output bandwidth	real or complex	output data rate/chan	usable bandwidth	sample rate	DUC or bypass	input bits resolution	real or complex	input data rate/chan	usable bandwidth
1	3.0 GHz	dec = 4	16 I + 16 Q	600 MHz	complex	3.0 GB/sec	600 MHz	-	-	-	-	-	-
2	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz	2.8 GHz	int = 2	16 I + 16 Q	complex	5.6 GB/sec	1120 MHz
3	2.8 GHz	dec = 4	16 I + 16 Q	560 MHz	complex	2.8 GB/sec	560 MHz	2.8 GHz	int = 4	16 I + 16 Q	complex	2.8 GB/sec	560 MHz
4	2.5 GHz	bypass	12	2.5 GHz	real	5.0 GB/sec	1000 MHz	-	-	-	-	-	-
5	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz	2.0 GHz	int = 2	16 I + 16 Q	complex	4.0 GB/sec	800 MHz
6	2.0 GHz	bypass	14	2.0 GHz	real	4.0 GB/sec	800 MHz	2.0 GHz	int = 2	16	real	2.0 GB/sec	400 MHz

Rationale for Each Mode

Mode 1: Maximum A/D sample rate of 3 GS/s, but the DDC must be used. D/A cannot operate at this sample rate.

Mode 2: Maximum sample rate for A/D and D/A both operating. DDC and DUC must be used, but D/A can generate twice the bandwidth of the A/D bandwidth.

Mode 3: Maximum sample rate for A/D and D/A both operating (like Mode 2), but now A/D and D/A bandwidths are the same

Mode 4: Maximum A/D useable bandwidth achieved with DDC bypass (RAW) output data and 12 bit resolution. D/A cannot operate in this mode.

Mode 5: Maximum useable signal bandwidth with A/D and D/A both operating. A/D is in bypass with 14 bit resolution. D/A uses DUC with interpolation of 2.

Mode 6. Like Mode 5 except D/A interpolates real samples instead of complex samples resulting in 400 MHz bandwidth and a simpler output anti-aliasing filter

General Notes

1. "Useable bandwidth" is equal to 80% of the Nyquist bandwidth
2. Anti-aliasing filters are required for A/D inputs and D/A outputs to ensure elimination of unwanted out-of-band signals per Nyquist criteria
3. Data rates shown are for the interfaces between the FMC module and the FPGA of the FMC carrier for each channel
4. By changing board support software, other operating modes are possible, including different decimations and interpolations
5. The sample rates shown for each mode are the maximum rates for that mode, but lower rates are also supported, with other parameters scaled appropriately
6. Only one mode is allowed at a time, which defines operations for both A/D and D/A