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# The Pentek Pipeline

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*A quarterly publication for engineering system design and applications.*

## In This Issue


- **Feature:** In an interview with ***Aerospace & Defense Technology*** magazine, Pentek's Vice President, Rodger Hosking, explains how software radio has evolved to play a critical role in military and aerospace electronic systems.

"Software radio technology now pervades an extensive range of mil-aero applications including radar, EW, communications, SIGINT, ELINT, countermeasures, weapons, missiles, monitoring, navigation, and tracking."
~ Rodger Hosking

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## The Inside Story on Software Radio

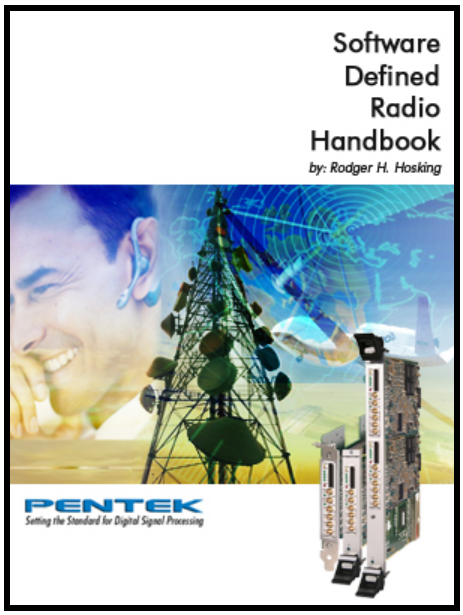
*Aerospace & Defense Technology interviews Rodger Hosking*

**A&DT: What is software radio and how did it get started?**

**Rodger:** Two critical technologies started to evolve rapidly in the 1970s. The first is data conversion technology that gave us ADCs (analog-to-digital converters) and DACs (digital-to-analog converters). The second is digital signal processing device technology that gave us DSP hardware chips. These enhanced microprocessors have dedicated multipliers, look-up tables, arithmetic units and memories to perform the necessary operations on sampled signals to and from DACs and ADCs at a given sample rate. Since these operations are controlled by software programs, once these DSPs and data converters were fast enough to convert and process radio frequency signals, the term "software defined radio" (or now simply "software radio") was coined.

**A&DT: Are software radios better than older analog radios?**

**Rodger:** Traditional analog radios used coils, capacitors, resistors, amplifiers, filters, diodes, mixers, and oscillators to acquire signals from an antenna, perform frequency translation, filter out unwanted signals, and perform demodulation of the desired signal. Because analog components are subject ➢




For a more detailed discussion of Software Defined Radio, download our *SDR Handbook* by clicking **here**.

to manufacturing tolerances, aging characteristics, and temperature dependency, analog radios for critical military applications must not only be carefully tuned and adjusted during manufacture, but also require periodic re-certification and calibration when deployed. Software radios replicate most of these same signal processing operations using DSPs, whose mathematically precise engines deliver consistent operation initially and over time.

**A&DT: Can I connect a software radio directly to an antenna?**

**Rodger:** Most software radios need some additional analog RF circuitry between the antenna and the ADC for amplifying and filtering the received radio signal before digitizing. If the radio signal frequency is too high for the ADC, the band of interest must be downconverted to a lower frequency IF signal. DAC analog output signals must usually be filtered and often upconverted from IF to RF before a power amplifier delivers the RF transmit signal to the antenna.

**A&DT: Were software radios adopted immediately?**

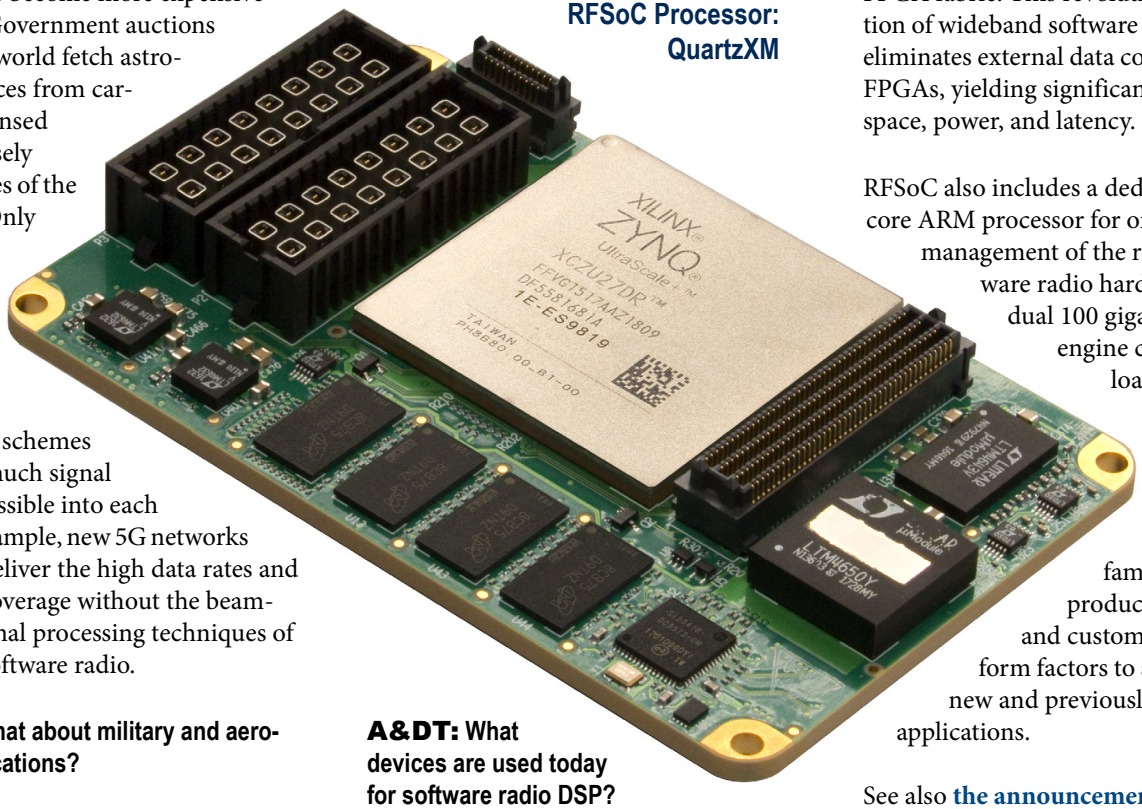
**Rodger:** It took a little time, but not too much. After introducing the world's first COTS digital receiver board product in 1992, Pentek started engaging with engineers who were expert RF radio designers and naturally quite skeptical of ADCs and DSPs. Once they saw that software radio performed the same signal processing functions as their analog designs, but using different hardware, they increasingly embraced the many benefits and new possibilities. Now, virtually all radios, entertainment electronics, communication devices, personal electronics, and video services across consumer, commercial and military applications use software radio technology.

**A&DT: Can't software radios do more than just replace analog radios?**

**Rodger:** One of software radio's most important benefits is in dramatically boosting the efficient use of the radio ➢

frequency spectrum. Like land, this finite resource has become more expensive over time. Government auctions around the world fetch astronomical prices from carriers for licensed use of precisely defined slices of the spectrum. Only software radio can implement the incredibly complex modulation schemes to pack as much signal traffic as possible into each slice. For example, new 5G networks could not deliver the high data rates and wide area coverage without the beamforming signal processing techniques of advanced software radio.

**Pentek's Model 6001 RFSoC Processor: QuartzXM**




**A&DT: What about military and aerospace applications?**

**Rodger:** Driven by the need for military superiority, software radio technology now pervades an extensive range of mil-aero applications including radar, EW, communications, SIGINT, ELINT, counter measures, weapons, missiles, monitoring, navigation, and tracking.

The key performance advantage of these new systems is often gained by innovative digital signal processing techniques to gain an exploitative edge across the entire electromagnetic spectrum.

**A&DT: What's the latest in software radio data converters?**

**Rodger:** As radio signal bandwidths increase to support soaring data rates and information content for commercial and military systems, data converters must keep pace with higher sampling rates. Monolithic ADCs and DACs now boast sample rates above 10 GS/sec to achieve receive and transmit bandwidths exceeding 4 GHz.

**A&DT: What devices are used today for software radio DSP?**

**Rodger:** Originally, DSPs were dedicated devices, but soon digital signal processing operations were performed on a wide range of processors including RISCs, bit slices, transputers, and graphics accelerators. Today, FPGAs (field programmable gate arrays) dominate software radio for defense electronics. Here, thousands of hardware-configurable DSP engines operating in parallel can be tailored for specific, compute-intensive tasks and real-time I/O data paths to significantly out-perform instruction-driven processors. FPGAs can also handle the complex timing for the triggered data acquisition and waveform generation needed for radar and EW systems.

**A&DT: What about the new Xilinx RFSoC devices?**

**Rodger:** RFSoC (RF System-on-Chip) integrates both essential elements of software radio in a single device: data converters and FPGAs. RFSoC includes eight 4 GS/sec 12-bit ADCs and eight 6.4 GS/sec 14-bit DACs, which are directly coupled to Xilinx's powerful UltraScale+ 16nm FPGA fabric. This revolutionary integration of wideband software radio resources eliminates external data converter links to FPGAs, yielding significant savings in space, power, and latency.

RFSoC also includes a dedicated quad-core ARM processor for on-board system management of the real-time software radio hardware. Lastly, a dual 100 gigabit Ethernet engine connects payload data between the RFSoC and system resources. Pentek offers its Quartz™ family of RFSoC products for 3U VPX and custom embedded form factors to achieve entirely new and previously-impractical applications.

See also **the announcement of our new SOSA aligned RFSoC board**! ❐

To gain a better appreciation of the capabilities of RFSoC and understand how to best use the advantages of this technology, download our FREE white paper by clicking **here**.

# Pentek's Paul Mesibov: A Key Contributor to Industry Standards

*The VITA Standards Organization (VSO) has started a "**VITA Personas**" segment on their website to highlight some of the people who contribute to shaping VITA standards.*

*The **VSO recently featured Paul Mesibov**, co-founder and Chief Technical Officer at Pentek, as one of their VITA Personas. What follows is taken from the VSO's profile of Paul.*

[Paul Mesibov] has over 35 years' experience in the electronics industry and oversees the design and implementation of Pentek's digital signal processing, software radio, and data acquisition products. He is currently an active member of **SOSA**, **PICMIG**, **VITA**, **PCI-SIG**, and **IEEE,** as well as a key contributor to several **ANSI** standards.

Prior to his current position, he was a design engineer for AP Circuit, Inc., designing active signal processing analog filters and Wavetek, Inc., designing benchtop signal processing filter products. He holds a bachelors and masters degree in Electrical Engineering from the City University of New York. Aside from Paul's engineering forte, he is also an accomplished musician.

VITA
Open Standards, Open Markets

## WORK WITH VITA

**VSO: Explain some of the work you're doing with VITA 49.0 (also known as VRT for VITA Radio Transport) and its recent companion standard, VITA 49.2.**

**Paul:** Having been involved in the development of VITA 49 since its inception, I participated in drafting several parts of the original standard and have continued as an active member of the working group to extend its scope and features. At Pentek, we've worked to add these VITA 49.0 protocol engines to several of products over the last eight years, including the latest **Quartz™ RFSoC product line**.

**VSO: What is the significance of the new packet classes added to VITA 49.2 in 2017?**

**Paul:** These new extensions add support for transmit signals so that precisely-timed waveforms can be generated by D/A converters for radar pulses, counter measures, and communication systems. They also add control packets that can control the operational parameters of receivers and transmitters as well as monitor status to verify proper operation.

For example, the **RFSoC products** mentioned generate VITA 49.0 header packets that are appended to data blocks acquired with A/D converters and digital down converters. The headers include metadata for the signals, including time-stamp, frequency, and bandwidth information. These packets are extremely useful for distributing radio signals across the network-based radio topologies that are now replacing the older, dedicated "stovepipe" architectures.

**VSO: Why is SDR (software-defined radio) an important component of embedded systems?**

**Paul:** SDR really means radio equipment whose operating modes are controlled by programming, rather than fixed circuitry, for a particular radio band or signal type. Specifically, SDR means that radio signals are digitized as "close" to the antenna as possible and the traditional sections of radios, like mixers, oscillators, filters and demodulators, are all performed by programmable and configurable digital signal processing blocks.

This allows common hardware elements to be re-purposed for a wide range of different signals and different applications. This offers a big savings in SWaP (size, weight and power), which is especially important in aircraft and unmanned vehicles. It also extends the useful life cycle of radio equipment because new features can often be added by software upgrades.

## WHY ENGINEERING?

**VSO: Did you always want to be an engineer? If so, why? If not, how'd you wind up here?**

**Paul:** When I was five I wanted to be a "builder." I spent the 1960s watching every NASA rocket launch. Looking back on some of the notebooks I have from when I was 12, it's clear that I liked robots, since I have a whole bunch of drawings showing how I could wire their motors. I ended up spending my teenage years playing electric guitar, which meant building up guitar amps from old radios. ➢

Next thing I knew, I was in a community college physics class on a field trip to the Princeton Plasma Physics lab visiting their fusion reactor. Someone asked if there were any electrical engineers in the group. That's when I knew what I wanted to do.

**VSO: What has surprised you the most about the work you do with embedded computing? (or engineering in general)**

**Paul:** That I'm still doing it. Seriously though, the surprising thing about electrical engineering is the range and scope of the learning to which a good engineer is exposed. After almost 40 years as an EE (electrical engineer), I know at least something about a wide range of engineering disciplines—not just those I studied in school. Most good EEs say the same thing.

**VSO: What is one of the biggest issues currently facing engineers?**

**Paul:** While the Internet has been a fantastic resource for engineering research—I'd never want to go back to the days of searching the IEEE Proceedings on microfiche—it is not a replacement for critical thinking. When there is more information than ever to sift through, the ability to put information in context has never been more important. I suppose that is good advice for everyone, not just engineers.

**VSO: What advice would you give to someone looking into this field of engineering?**

**Paul:** Most successful embedded systems engineers are hobbyists. Play with this stuff at home, too.

Whatever you decide to pursue, make sure you go to a place where there are mentors that you respect and that the culture of the organization promotes learning and intellectual growth. It's sometimes hard to know going in, but do what you can to find out. Working at the right place sets up your whole career.

**VSO: Off the cuff: Tell us your favorite joke.**

**Paul:** Q: What is the difference between hardware and software?

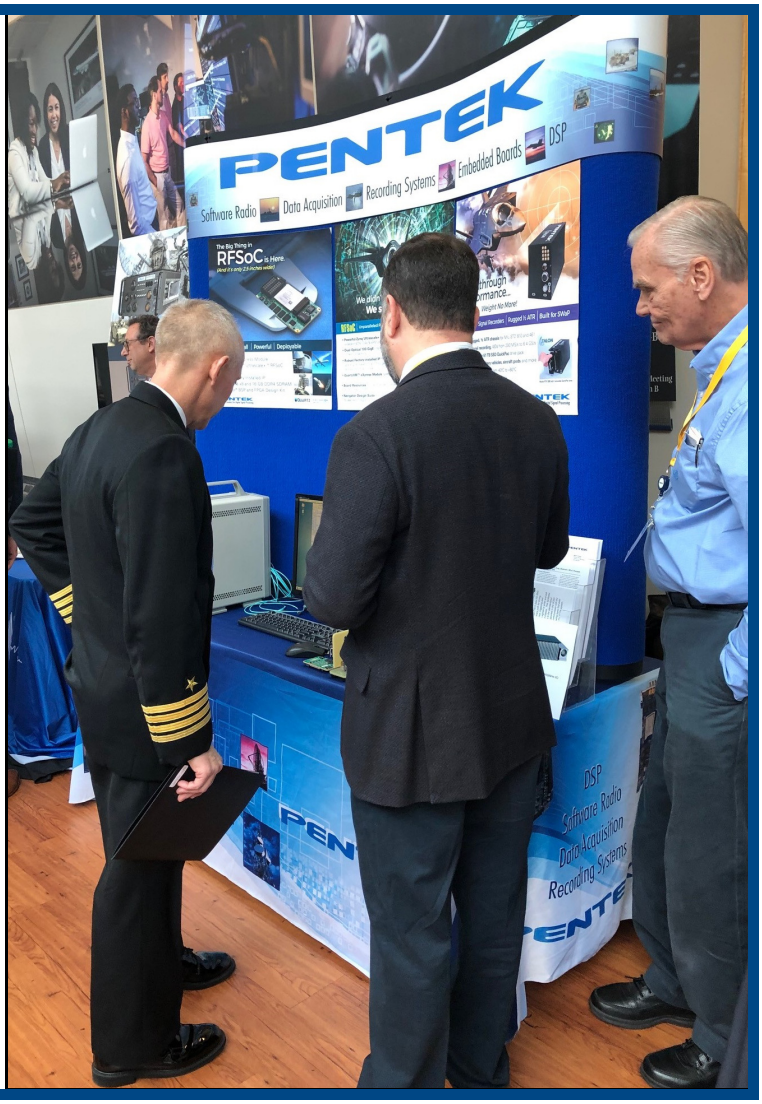
A: Hardware is a thing that if you play with long enough, it breaks. Software is a thing that if you play with long enough, it works. ❐

## Pentek Participated in the Tri-Service Open Architecture Interoperability Demonstration (TSOA-ID) on January 29, 2020

The TSOA-ID was sponsored by Representative Commands from Branches of the United States Armed Services and hosted by Georgia Tech Research Institute at the GTRI Conference Center in Atlanta, Georgia.

Joining Tri-Service representatives in demos were industry vendors (including Pentek) that represented the Industry and Government partnership with: HOST, SOSA™, CMOSS and VITA Standards development organizations.

Shown in the photo on the right: Captain McDowell and his counterparts are key partners in the tri-service open architecture ecosystem. He and Paul Mesibov of Pentek discussed Pentek's SOSA aligned products demonstrated at the TSOA-ID event. The future promises more cooperation.



# Pentek's New Quartz RFSoC Board is Aligned with the Technical Standard for the SOSA Reference Architecture

Pentek recently introduced the Quartz™ **Model 5550**, an eight-channel A/D and D/A converter, 3U OpenVPX™ board based on the Xilinx® Zynq® UltraScale+ RFSoC and aligned to the **SOSA Technical Standard**. The Model 5550 is ideal for many communications, electro-optical, electronic warfare, radar, and signals intelligence applications.

- Supports Xilinx Zynq UltraScale+ RFSoC FPGAs
- 16 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3)
- 40 GigE Interface
- Optional **VITA** 67.3D optical interface for backplane gigabit serial communication
- Dual 100 GigE UDP interface
- Compatible with several **VITA** standards including: VITA 46, VITA 48, VITA 67.3D,VITA 65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

***"The Model 5550 is leading the industry in the rollout of products developed in alignment with the Technical Standard for the SOSA Reference Architecture,"*** said Bob Sgandurra, director of Product Management at Pentek. ***"Pentek continues to be very active in the development of the SOSA Technical Standard and we are now demonstrating our commitment with supporting products and demonstrations."***

SOSA™
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A key development breakthrough was the decision to implement connector technology that enables one of the major goals of SOSA reference architecture: backplane only I/O. **Model 5550** incorporates the ANSI/**VITA 67.3D** VPX Backplane Interconnect standard for both coaxial RF and optical I/O. In addition, Model 5550 includes a 40GigE interface and a shelf-management sub-system that are also required in the SOSA reference architecture.

Pentek's modular approach to hardware and software enables quick adaptation to new and changing customer requirements. The **Model 5550** uses the **Model 6001** QuartzXM eXpress module containing the RFSoC FPGA and all needed support circuitry implemented on a carrier module designed specifically to align with the technical standard for the SOSA reference architecture. This allows easy upgrades to third generation RFSoC modules when available.

**Model 5550 with cover removed to show Model 6001 QuartzXM Module**

QUARTZ

## Factory Installed IP Advances Development

The Model 5550 is pre-loaded with a suite of Pentek IP modules to provide data capture and processing solutions for many common applications. Modules include DMA engines, DDR4 memory controller, test signal and metadata generators, data packing, and flow control. The board comes pre-installed with IP for triggered waveform and radar chirp generation, triggered radar range gate selection, wideband real-time transient capture, flexible multi-mode data acquisition, and extended decimation. For many applications, the Model 5550 can be used out-of-the-box with these built-in functions, requiring no FPGA development.

## Data Conversion and Analog I/O

The front end accepts analog IF or RF inputs on eight coax connectors located within a VITA 67.3D backplane connector. After balun coupling to the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x, ➢

and 8x decimation and independent tuning. The A/D digital outputs are delivered into the RFSoC programmable logic and processor system for signal processing, data capture, or for routing to other resources. A stage of IP-based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

Eight 4 GSPS, 14-bit D/A converters deliver balun-coupled analog outputs to a second VITA 67.3D coaxial backplane connector. Four additional 67.3D coaxial backplane connections are provided for clocks and timing signals.

## Expandable I/O

The Model 5550 also uses the VITA-67.3D backplane connector for eight 28 Gb/sec duplex optical lanes to the backplane. With two built-in 100 GigE UDP interfaces or a user-installed serial protocol in the RFSoC, the VITA-67.3D backplane interface enables gigabit communications independent of the PCIe interface.

## Navigator Design Suite

Pentek's **Navigator Design Suite** includes: Navigator FDK (FPGA Design Kit) for custom IP and Navigator BSP (Board Support Package) for creating host software applications.

The **Navigator FDK** includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. All source code and complete documentation is included. Developers can integrate their IP along with the factory-installed functions or use the Navigator kit to replace the IP with their own. The Navigator FDK Library is AXI-4 compliant, providing a well-defined interface for developing custom IP or integrating IP from other sources.

The **Navigator BSP** supports Xilinx's PetaLinux on the ARM processors. Users work efficiently using high-level API functions, or gain full access to the underlying libraries including source code. Pentek provides numerous examples to assist in the development of new applications.

## For more information ...

**For more information** about **Model 5550, click here.** You also can email us at sales@pentek.com, contact **your local representative**, or contact Pentek directly [+1 (201) 818-5900].

**To receive updates about SOSA** and Pentek's SOSA aligned products, subscribe to our new email list by **clicking here**.

**To listen to a podcast about SOSA**, **click here**. McHale Report editors John McHale and Emma Helfrich, and their guest, Rodger Hosking, discuss SOSA, TSOA-ID, and artificial intelligence.

**Take a look at Pentek's new SOSA information pages! Click here to go there.**

# Pentek Announces a 6.4 GHz A/D and D/A Jade 3U VPX Module for Wideband Defense, Radar, and Communication Applications

Pentek recently introduced the newest member of the Jade® family of high-performance data converter 3U VPX modules based on the Xilinx® Kintex® Ultrascale™ FPGA. The **Model 54141A** is a dual channel analog-to-digital and digital-to-analog converter with sample rates up to 6.4 GHz. Programmable DDCs (digital downconverters) and DUCs (digital upconverters) support connections to IF or RF signals.

- Exceptional dynamic range and analog signal integrity
- Xilinx Kintex UltraScale FPGAs
- 1-channel mode with 6.4 GHz, 12-bit A/D
- 2-channel mode with 3.2 GHz, 12-bit A/Ds
- Compatible with several **VITA** standards, including: VITA 66.5 and VITA 67.3C
- Supports **VITA** 49.2 VITA Radio Transport standard
- Programmable DDCs
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs
- 5 GB of 2400 MHz DDR4 SDRAM
- uSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
- Navigator Design Suite

***"The 54141A combines our popular 71141A XMC module with a 3U VPX carrier, yielding a powerful, forward-looking package for very wideband communications or radar applications that require advanced I/O resources,"*** said Rodger Hosking, vice-president of Pentek, Inc.

Not only does the Model 54141A comply with the VITA 65.0 3U VPX specification, it also offers flexible analog and digital interface options for the VPX P2 backplane connector to meet system-specific requirements. In addition to its PCIe Gen.3 x8 interface on the VPX P1 connector, it is possible to add up to eight more gigabit serial lanes connected directly to the FPGA for supporting user-installed protocols.

**Model 54141A**

The Model 54141A supports the emerging VITA 66.5 optical interconnect standard by providing four optical duplex lanes to a mating spring-loaded backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the interface enables high-bandwidth digital communications between boards or chassis independent of the PCIe interface.

For flexibility across different I/O requirements, the board can be optioned to support VITA 67.3C. This provides analog signal routing through the VPX backplane to replace front panel connectors for RF In/Out, Sample/Reference clocks, and Gate/Trigger/Sync/PPS signals. This option is often required in ruggedized deployments and for simplifying unit field replacements and upgrades.

## A/D Stage and Digital Downconverter

The Model 54141A uses the Texas Instruments ADC12DJ3200 12-bit A/D converter with an input bandwidth of 6 GHz, which operates in single-channel interleaved mode with a sampling rate of 6.4 GHz or in dual-channel mode with a sampling rate of 3.2 GHz.

## Digital Upconverter and D/A Stage

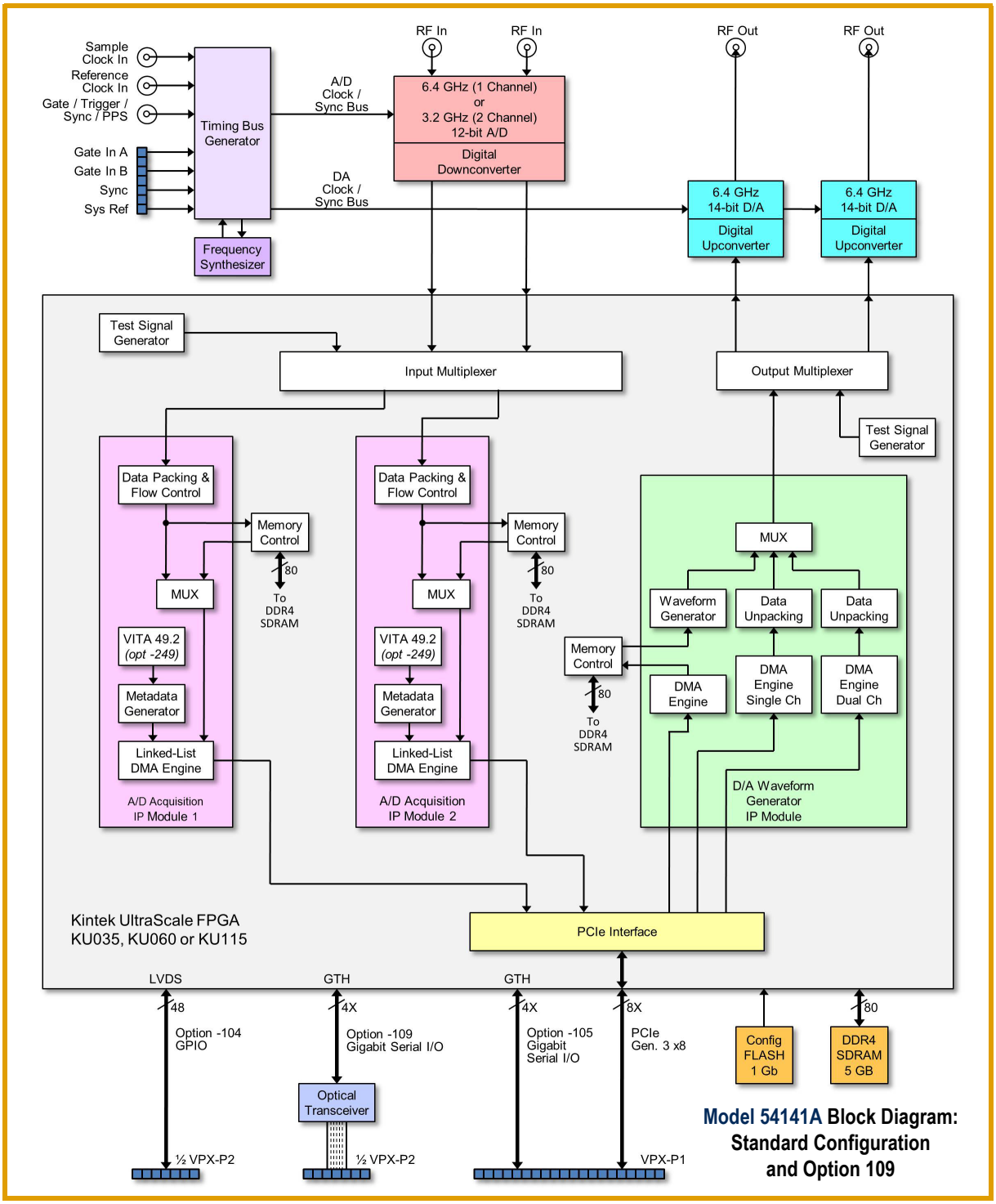
A Texas Instruments DAC38RF82 D/A with DUC accepts a baseband real or complex data stream from the FPGA and delivers it to the interpolation, upconversion and dual D/A stages for output signals up to 4 GHz. The two 6.4 GHz 14-bit D/As pair well with the dual input channels while delivering more than twice the output performance of previous generations of Pentek products. ➢

## Performance IP Cores

The Model 54141A includes two A/D acquisition modules and a D/A waveform generation IP module. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe Gen.3 x8 interface complete the factory-installed functions. An optional VITA 49.2 data transport protocol IP module conveys digitized signal metadata for signal acquisition and processing elements in communication, radar or storage systems. System integrators get to market with less time and risk, because the Model 54141A can provide a complete acquisition/generation solution, often without the need to develop FPGA IP.

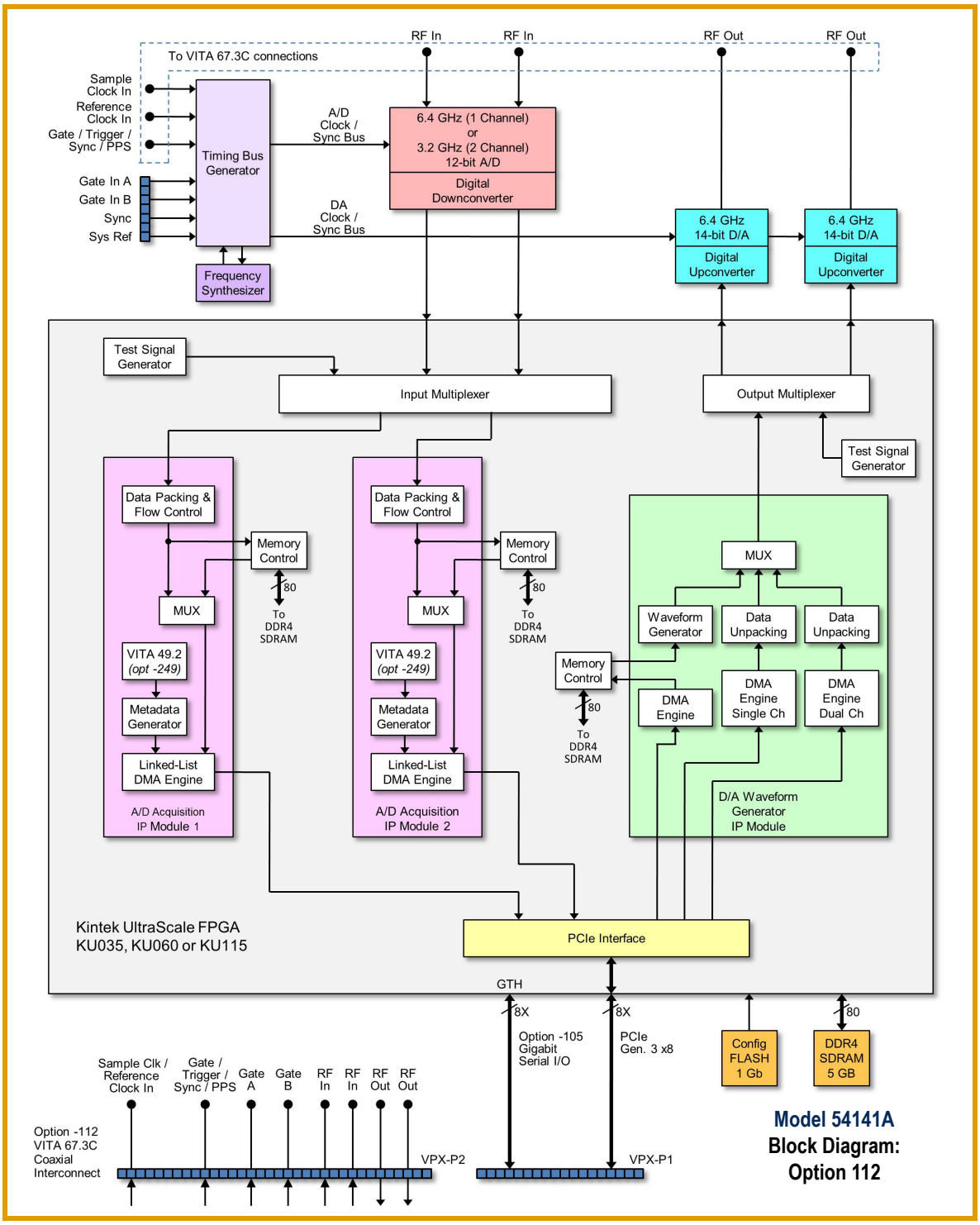
## The Jade Architecture

The Pentek Jade Architecture is based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by more than 50% ➢




**Model 54141A Block Diagram: Standard Configuration and Option 109**

with an equally impressive reductions in cost, power dissipation, and weight. As the central feature of the Jade Architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. A 5 GB bank of DDR4 SDRAM is available to the FPGA for custom applications. The x8 PCIe Gen 3 link can sustain 6.4 GHz data transfers to system memory. Eight additional gigabit serial lanes and LVDS general purpose I/O lines are available for custom solutions. The **Navigator Design Suite** enables streamlined IP development.

## For more information ...

For more information about **Model 54141A, click here.** You also can email us at sales@pentek.com, contact **your local representative**, or contact Pentek directly [+1 (201) 818-5900]. ❐