

Optimum Data Flow Solutions for High-Performance Systems

The most difficult problem for designers of high-performance, real-time digital signal processing systems is simply moving data within the system. Invariably, the problem is caused by data throughput limitations.

Many traditional methods of handling I/O tasks are no longer viable because they can't keep up with the speeds of new DSP and RISC processors. To improve system efficiencies, several new techniques to support fast data movement throughout the system have been created. Direct connections using private, high-speed data paths like those provided by mezzanines, front panel serial and parallel interfaces, and backplane fabrics can eliminate or significantly reduce data flow bottlenecks and arbitration for shared resources.

New Processor I/O Demands

The ability to take maximum advantage of the newest RISC and DSP processors in high-performance, open-architecture embedded systems depends entirely on how well connected they are to each other and to system I/O devices.

During the last few years, the industry has witnessed the introduction of several fast DSP and RISC processors with impressive benchmarks for popular algorithms and sophisticated hardware engines for caching, moving data, and addressing. These processors also support external data bus speeds that outstrip virtually every backplane available.

To better understand the scope of supporting these new DSP and RISC devices, Figure 1 shows a few metrics for data transfer speeds. As an example, the Texas Instruments TMS320C6203 DSP executes eight 32-bit instructions

PROCESSOR	21160	C6701	C6201	C6203	MPC7400
No. of Buses	1	1	1	2	1
Address Bus Width	32	24	24	24	32
Data Bus Width	64	32	32	32+32	64
Bus Cycle Time	15 nsec (66 MHz)	6 nsec (167 MHz)	5 nsec (200 MHz)	3.3 nsec (300 MHz)	7.5 nsec (133 MHz)
Bus I/O Rate (MB/sec)	528	667	800	1800	1067

Figure 1. Data Transfer Speeds for New DSP and RISC Processors

in parallel within a 3.33 nsec instruction cycle time, yielding 2400 MIPS operation. An on-chip multiple-path ALU and four-channel DMA controller are coupled to support extremely high-speed I/O peripherals. With dual 32-bit parallel data buses, it can move data to I/O devices at a combined speed of 1800 MB/sec!

The new Motorola G4 AltiVec MPC7400 PowerPC running with a 400 MHz clock is capable of performing 20 operations per cycle. Using its external 64-bit data bus, it can handle peak I/O rates to peripherals at 1067 MB/sec.

For these processors, the speed of the computing engine may no longer be the critical path in the real-time equation. Instead, some of these recent gains in computational power can be quickly sacrificed due to bottlenecks in moving data to and from peripheral devices.

Mezzanine Buses

Mezzanine buses offer alternative parallel data paths to the common backplane in bus systems and can dramatically help improve real-time performance in several ways. First, mezzanine buses can provide a direct dedicated data path between system peripherals and the processor, so that

data transfers can be guaranteed to meet real-time demands. Second, the data transfers on the backplane bus are reduced, making this bus more available for other traffic. And finally, since there can be multiple mezzanine buses within a system, the aggregate data transfer rates can be increased quite dramatically and in a modular manner. A few popular, high-speed mezzanines include PMC (PCI Mezzanine Card) and VIM (Velocity Interface Mezzanine). Figure 2 provides data transfer speeds for some mezzanine standards.

PMC has gained the support of virtually every board manufacturer in the high-end system bus community, first with VMEbus vendors, and now increasingly with Compact PCI vendors. The PMC module is attached to the carrier board using two, three or four 64-pin compact connectors, depending on the application. The PMC specification allows for direct connection through the front panel of the VME board. A separate PMC front panel can accommodate any specialized I/O connectors required by the module. Most PMC modules utilize the 32-bit interface and are capable of moving data in block transfers at 132 MB/sec. ➤

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Leading the performance race, the VIM mezzanine specification was developed to meet the needs of new high-speed processors like the Texas Instruments C6000 and the Motorola PowerPC. The VIM specification developed by Pentek, provides a dedicated 400 MB/sec data channel to each of four processors on a quad processor 6U VMEbus or CompactPCI board. Four 160-pin processor node connectors allow peripherals to deliver data directly to the private resources of each processor and include three types of electrical interface: high-speed parallel data, serial data, and control and status.

Some VIM module functions currently available include digital receivers and transmitters, high-speed A/D converters, and FPDP and RACEway interfaces. VIM modules can also be custom-designed using the design specification available free of charge from Pentek. In all configurations, custom or off-the-shelf, the processor board and attached VIM modules occupy the same single VMEbus slot. The obvious benefits are flexibility, higher density, lower cost and much faster I/O paths.

Front Panel I/O

As an alternative to using backplanes and mezzanines, several front panel data interconnect schemes have evolved which serve to reduce backplane traffic by sending data between boards using high-speed parallel and serial links. These include Front Panel Data Port (FPDP) and front-panel serial ribbon cables.

FPDP, an ANSI standard, provides a 32-bit parallel front panel bus between two or more VME boards. It is a unidirectional, synchronous bus providing well-defined data transfer speeds and delivers data at either 80 MB/sec or 160 MB/sec. Now in use by dozens of manufacturers, FPDP has proven itself as a simple, fast and inexpensive means for moving high-speed data between system components. A new version of FPDP is now being proposed which delivers 400 MB/sec performance.

MEZZANINE	IND. PACK	MIX	PMC	VIM
Data Bus Width (bits)	16	32	32/64	32
Bus Cycle Time (nsec)	250	100	30	10
Bus Cycle Rate (MHz)	4	10	33	100
I/O Bandwidth (MB/sec)	8	40	132/264	400
Buses per VME Slot	4	1	1	4
I/O Bandwidth per Slot (MB/sec)	32	40	132/264	1600

Figure 2. Data Transfer Speeds for Mezzanines

Backplane I/O

Front panel cable buses solve many types of interconnection problems for the system designer but suffer from the complication of having to fabricate, document, install and maintain cables of various types. For applications, where high availability is a significant issue, front panel connections of any type are undesirable.

A better solution for very high-speed I/O movement in applications is RACEway, created by Mercury Computer. RACEway is a backplane interconnection fabric that allows multiple boards to send and receive data simultaneously

at rates far exceeding the basic VMEbus specification.

RACEway uses a separate overlay printed circuit board assembly which is attached to the VMEbus backplane, using mating sockets that engage the 64 user defined tail pins on the P2 connectors. It joins as few as two and as many as twenty VME slots. Each RACEway path operates synchronously at a clock rate of 40 MHz providing a data transfer rate of 160 MB/sec. Just now becoming available is the RACE++ technology which operates at a clock speed of 66.66 MHz and delivers 267 MB/sec transfers. ➤

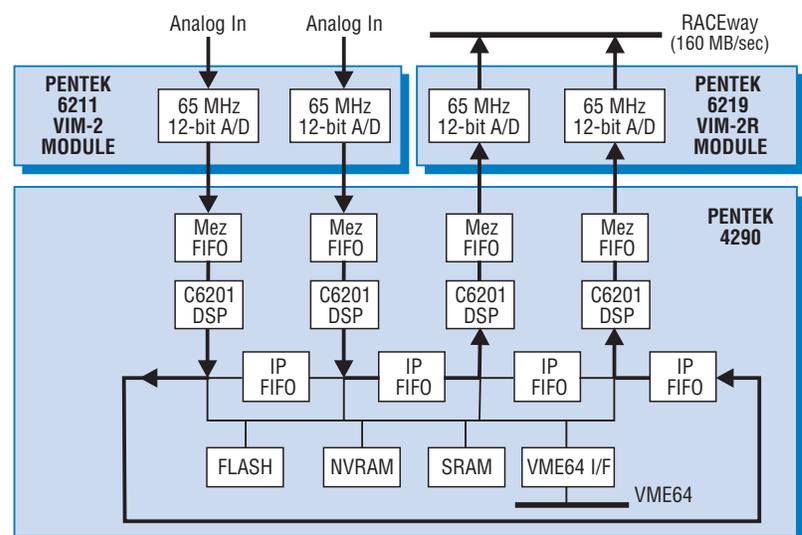


Figure 3. Quad C6201 DSP with VIM Mezzanines for A/D and RACEway

32-Channel Digital Receiver VIM-4 Module

[From page 4]

which perform various modes of data packing, formatting and channel selection. The A/D outputs are also connected directly to the FPGAs so that wideband A/D data can be delivered directly to the DSP board, bypassing the digital receivers.

Optionally available design kits will allow the FPGAs to be configured by the user for implementation of custom pre-processing functions such as convolution, framing, and pattern recognition.

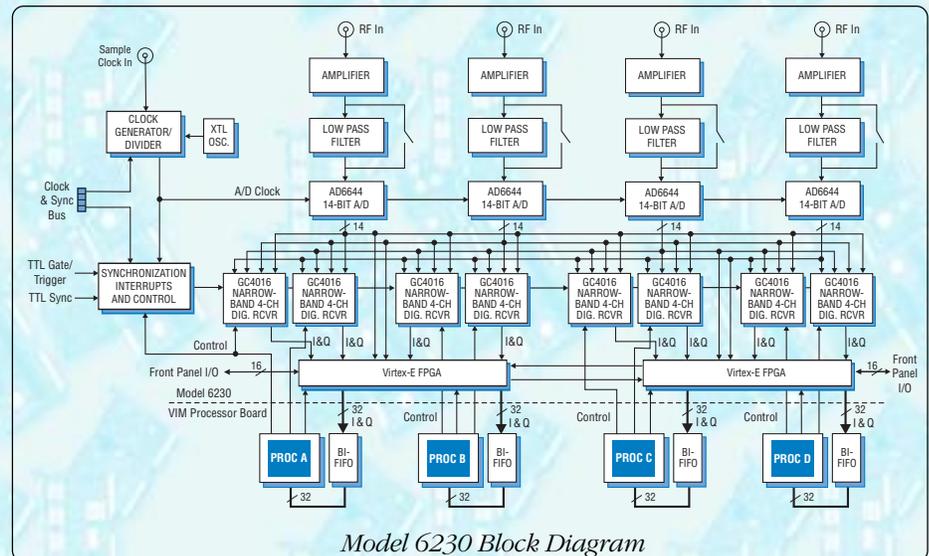
VIM Processor Interface

The FPGA outputs are connected directly through the VIM mezzanine interface to the 32-bit BI-FIFO on the VIM processor board where it is buffered for efficient block transfers into the DSP. The DSP can control the programmable registers on its GC4016's and initiate sync bus functions.

Pentek's ReadyFlow Board Support Libraries allow high-level programming to speed development tasks.

For more information on the Model 6230 visit our website at:

<http://www.pentek.com> □



Model 6230 Block Diagram

Putting it All Together

With these high-speed interfaces available to meet the needs of the new generation of DSP and RISC chips, we will now show how they can be implemented on a multiprocessor board. As shown in Figure 3, a very high-performance data acquisition and signal processing system can be built using the VIM mezzanine and RACEway interfaces.

The Quad 'C6201 DSP processor board is equipped with two VIM mezzanine modules. The dual 65-MHz A/D VIM module features two channels of 65 MHz 12-bit A/D conversion delivering two parallel data streams of 130 MB/sec each into two processor nodes. Using dedicated interprocessor FIFOs, pre-processed data is transferred across two processor nodes for final processing. Finally, packets of processed data are sent through the VIM mezzanine RACEway interface for delivery to a RACEway target via the 160 MB/sec RACEway backplane. Each of these data transfers takes place using no shared resources, completely eliminating data flow conflicts normally found in more traditional architectures. □

Pentek's System Configuration Services (SCS)

Responding to customer requests to deliver system components already installed and configured within the card cage, Pentek has formed a separate engineering group to provide System Configuration Services (SCS) at very reasonable prices. The services are based on a fixed fee which is quoted in advance and can be included in the purchase order for the boards that form your system.

What does SCS Provide?

SCS provides a tested system, configured to your needs, all ready for application development. Depending on your system requirements, SCS may include some or all of the following services:

- ❖ Installation of the purchased hardware into a VMEbus enclosure
- ❖ Design, build and test of custom interconnecting cables
- ❖ Installation and test of Pentek software, including ReadyFlow and SwiftNet
- ❖ Installation and test of third-party software purchased through Pentek
- ❖ Functional test of the entire system

- ❖ System test software code tailored to match your application, giving you a valuable "head start"
- ❖ Custom system documentation

What Are the Benefits?

- ❖ Your system is configured by experts
- ❖ You can start application development immediately
- ❖ Jumpers and cables are installed and tested
- ❖ Signal flow paths are verified
- ❖ Example source code for your application is included
- ❖ Detailed technical documentation is included
- ❖ The work is very reasonably priced
- ❖ You can complete your system faster
- ❖ You can expect quick turnaround

With increasing pressure to shrink development schedules, system engineers need to spend their valuable time focusing on application-specific tasks, rather than installing jumpers and cables. Call us to see what SCS can do for you. For a turnkey system solution, contact companies such as DSPCon at 908-722-5656. □



32-Channel Digital Receiver VIM-4 Module

Unit Also Includes Quad A/D and FPGAs for Signal Preprocessing

Model 6230

Intended for Pentek's VIM-compatible processor boards, Model 6230 is a VIM-4 module that includes four A/D converters, a 4-input 32-channel narrowband digital receiver, and two FPGAs (field programmable gate arrays) for signal preprocessing tasks, such as formatting and data packing.

Front End

Model 6230 accepts four analog RF inputs on front panel SMA connectors in the range of DC to 90 MHz to support direct IF undersampling. Each input is amplified and then, optionally, lowpass filtered to avoid aliasing of baseband signals.

The four inputs are then digitized by an AD6644 14-bit A/D converter,

which is currently capable of operating at sample rates up to 65 MHz (80 MHz devices are in development). The A/D converter clock can be driven from an internal 64 MHz crystal oscillator or from an external clock supplied through a front panel SMA connector.

Digital Receivers

The 6230 includes eight Graychip GC4016 quad narrowband digital receiver chips. The maximum input sampling rate for the GC4016 is 80 MHz. Each device includes four independently tuned receiver channels capable of center frequency tuning from DC to 32 MHz, and with output bandwidths ranging from 3.2 kHz to 1.6 MHz (for 64 MHz sample clock).

The GC4016 accepts four 14-bit parallel inputs from the four A/D converters.

A crossbar switch inside each GC4016 allows all 32 receiver channels on the board to select any of the four A/D inputs for flexible switching.

Synchronization

Front panel clock and sync buses allow one 6230 to act as a master, driving the sample clock out to a front panel cable bus using LVDS (low-voltage differential signaling). Multiple slaves can then be synchronized with the master.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and FIFO data collection on multiple 6230's.

FPGA

The 32 receiver outputs are delivered to two Xilinx Virtex-E FPGAs ▶

- ▶ The latest datasheets
- ▶ The latest product brochures
- ▶ Technical overviews
- ▶ Seminar locations and more...

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Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458-2311



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