New!

Model 7851

256-Channel DDC with Four 200 MHz, 16-bit A/Ds - x8 PCIe

ReadyFlow Board Support Package

Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x8 wide
- Built-in fan for added cooling
- 256 DDC channels
- Four 200 MHz 16-bit A/Ds
- Independent tuning for each channel
- DDC decimation from 128 to 1024 in steps of 64
- Independent decimation for each bank
- Each bank independently selects one of four A/Ds
- User-programmable 18-bit FIR filter coefficients
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7851 is a high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds. The A/D converters are supported by a high-performance 256-channel installed DDC (digital downconverter) IP Core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The 7851 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 7851 SX95T FPGA employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the attached four A/Ds as the input source for each DDC bank. In this way, many different configurations can be achieved including one A/D driving all 256 DDC channels and each of the four A/Ds driving its own DDC bank.

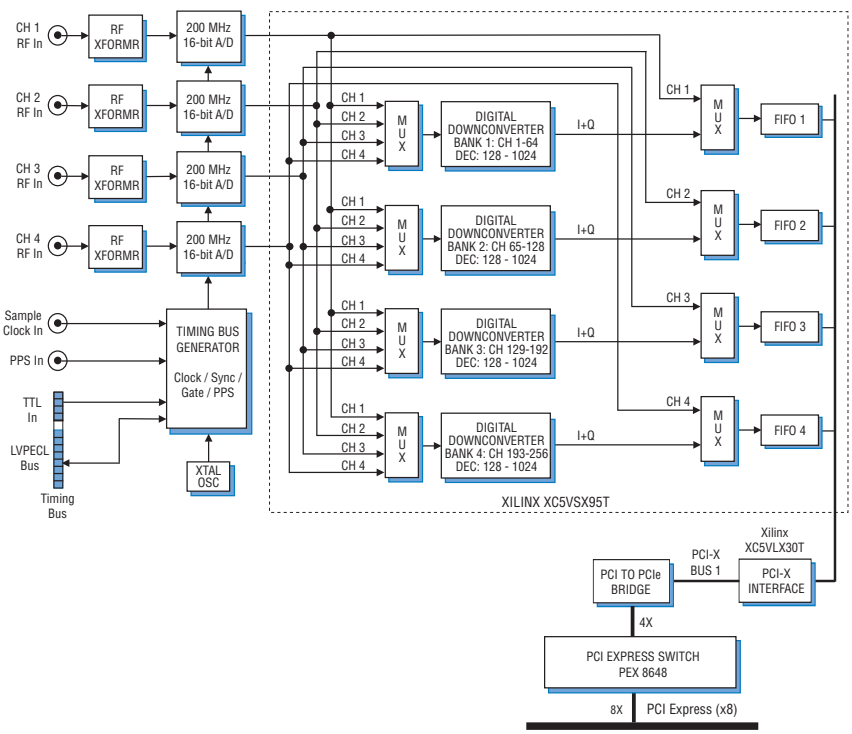
Each of the DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Decimation and Filtering

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled with each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank. ➤



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➤ Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7851 architecture includes a flexible timing and synchronization circuit for the bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connectors allows multiple modules to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7851s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. More modules can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7851 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with a 4X connection provided to the 64-bit PCI-X interface.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Internal Clock:** 200 MHz crystal osc.
- **External Clock:** 10 to 200 MHz
- **Resolution:** 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock
- **Type:** Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array
- **Processing FPGA:** Xilinx Virtex-5 XC5VSX95T dedicated to digital downcoverters and output
- **Interface FPGA:** Xilinx Virtex-5 XC5VLX30T dedicated to the PCI interface

PCI to PCIe Interface
- **PCI-X Bus:** 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz
- **DMA:** 4 channel demand-mode and chaining controller per PCI bus
- **PCIe Interface:** Gen. 2, x8 width
- **PCIe Ports:** one 4X port to PCI-X bus
  one 8X port to PCIe motherboard

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7851	256-Channel DDC with four 200 MHz, 16-bit A/D - Half-length x8 PCIe
Options:	
-731	Two-slot heat sink

Contact Pentek for additional available options.

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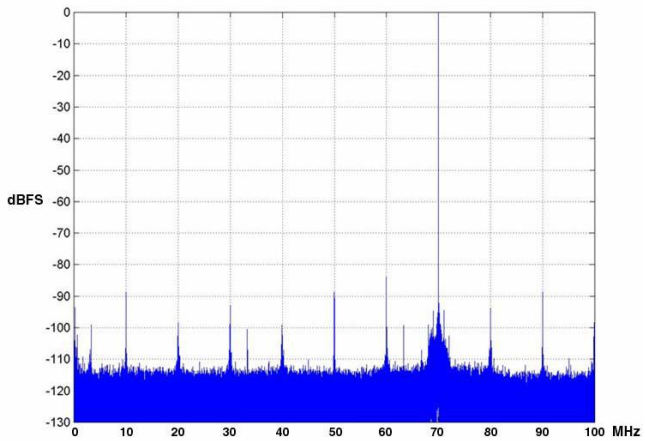
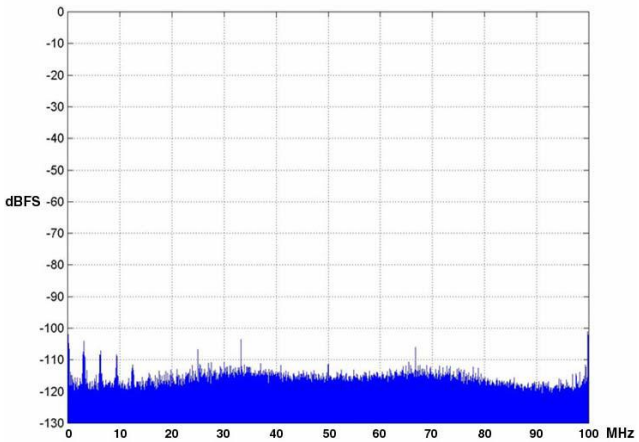
A/D Performance

Spurious-Free Dynamic Range



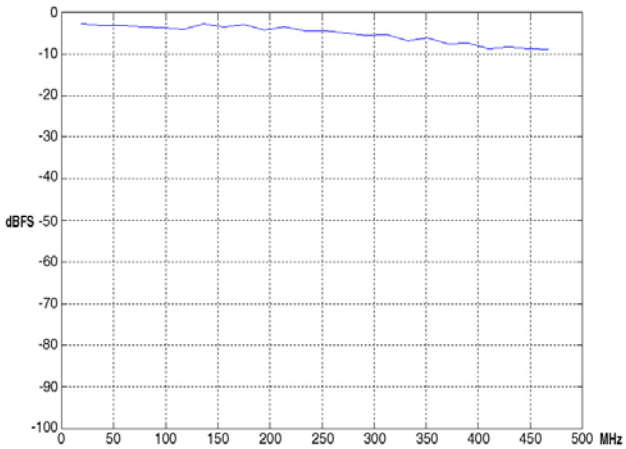
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup



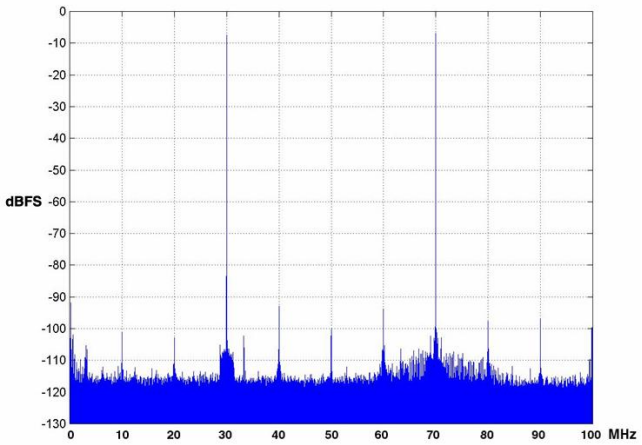
f_s= 200 MHz, Internal Clock

Input Frequency Response



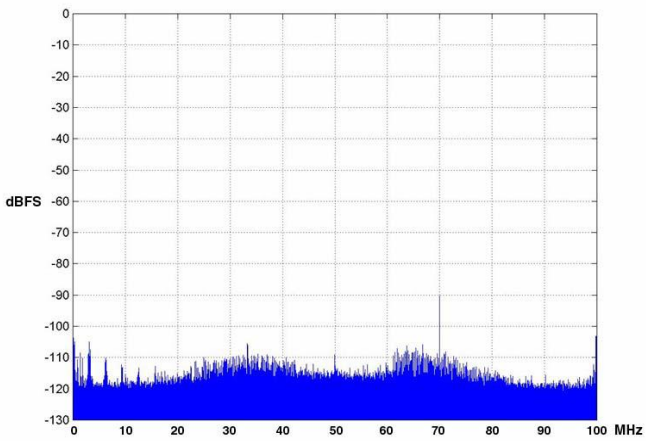
f_s= 200 MHz, Int. Clock

Two-Tone SFDR



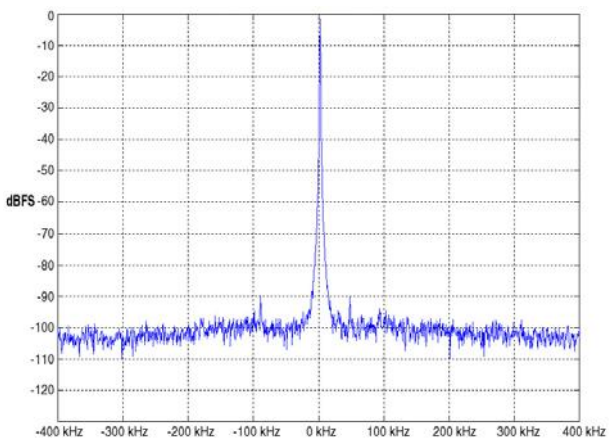
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk



f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz



f_s= 200 MHz, Int. Clock