New!

Model 52865

2-Ch 200 MHz 16-bit A/D Channelizer, 762 Narrowband DDCs, 4 Wideband DDCs, Kintex UltraScale FPGA - 3U VPX

Model 52865 Commercial (left) and rugged version

JADE NAVIGATOR Board Support Package

Features

- Complete software radio receiver solution for extremely high-channel-count applications
- Uses Xilinx Kintex UltraScale KU035 FPGA
- Two 200 MHz 16-bit A/Ds
- Four wideband DDCs (digital downconverters)
- Up to 762 narrowband DDCs
- Sample clock generation and synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 52865 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Board Support package, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing applications.

The 52865 is a two channel data converter with a total of 766 programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution for extremely high-channel-count systems.

It includes two A/Ds, a complete multi-board clock and sync section, eight banks of channelizer-based DDCs and resampling filters. The PCIe Gen.3 x4 interface is capable of sustained data transfers to system memory of over 3 GB/sec.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52865 factory-installed functions include two A/D acquisition IP modules for simplifying data capture and transfer.

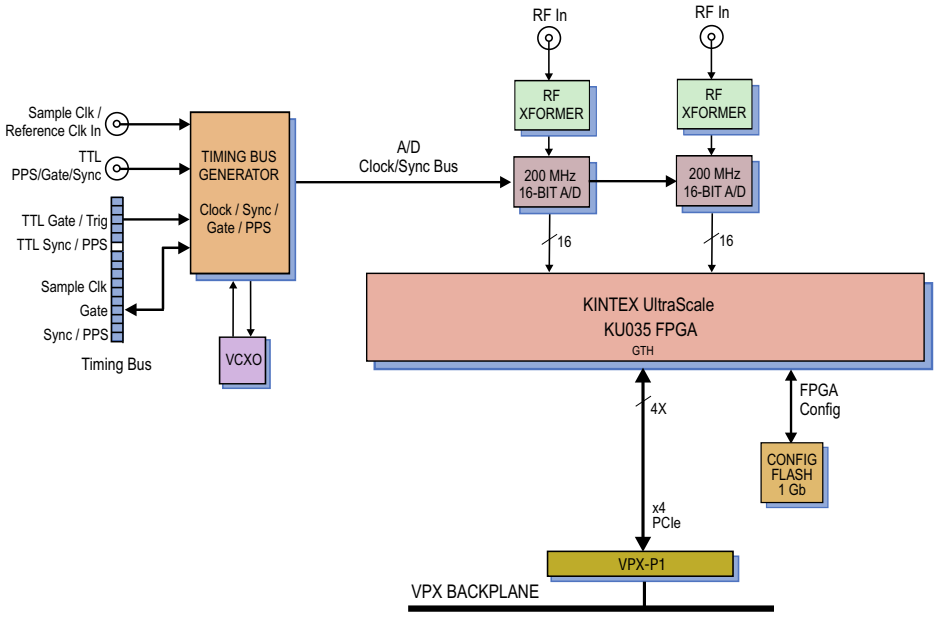
Each acquisition IP module contains a powerful, programmable DDC IP core and a controller for all data clocking, triggering, and synchronization functions.

From each of the two acquisition modules, A/D sample data flows into identical IP modules consisting of banks of wideband and narrowband DDCs. Finally, data is delivered to four DMA controllers and then to the PCIe Gen. 3 x4 interface.

These complete the factory-installed functions and enable the 52865 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale KU035 FPGA handles all of the control, timing, data formatting, and DSP operations for the channelized DDCs and is highly optimized to maximize resource utilization and reduce power dissipation. Because of its extremely advanced FPGA design, no Navigator FDK is offered for the 52865 for customers to modify the FPGA IP. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

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A/D Acquisition IP Modules

The 52865 features two A/D Acquisition IP Modules for easily capturing and moving data.

Each IP module has an associated DMA engine for easily moving DDC data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC Resources

Samples from the two A/D converters flow into two identical blocks, each containing one bank of two wideband DDCs and three banks of narrowband DDCs, as shown in the block diagram below.

Wideband DDCs

The four wideband DDCs can be set for decimation values between 8 and 128 in steps of 4, providing usable output bandwidths from 1.25 MHz to 20 MHz for a sample rate, f_s, of 200 MHz. Because all four wideband DDCs within the 52865 feed the same DMA controller #1, all wideband DDCs must use the same decimation factor.

Each DDC delivers an output stream consisting of 16-bit I + 16-bit Q complex samples at a rate of f_s/N. Four samples, one from each of the wideband DDCs, are interleaved in the output stream.

All four wideband DDCs can be independently tuned across the range from 0 Hz to f_s with 32 bits of resolution.

Narrowband DDCs

Each of the six narrowband DDC banks can be configured to operate in three different modes, where each mode provides a different quantity of DDC channels and range of decimations.

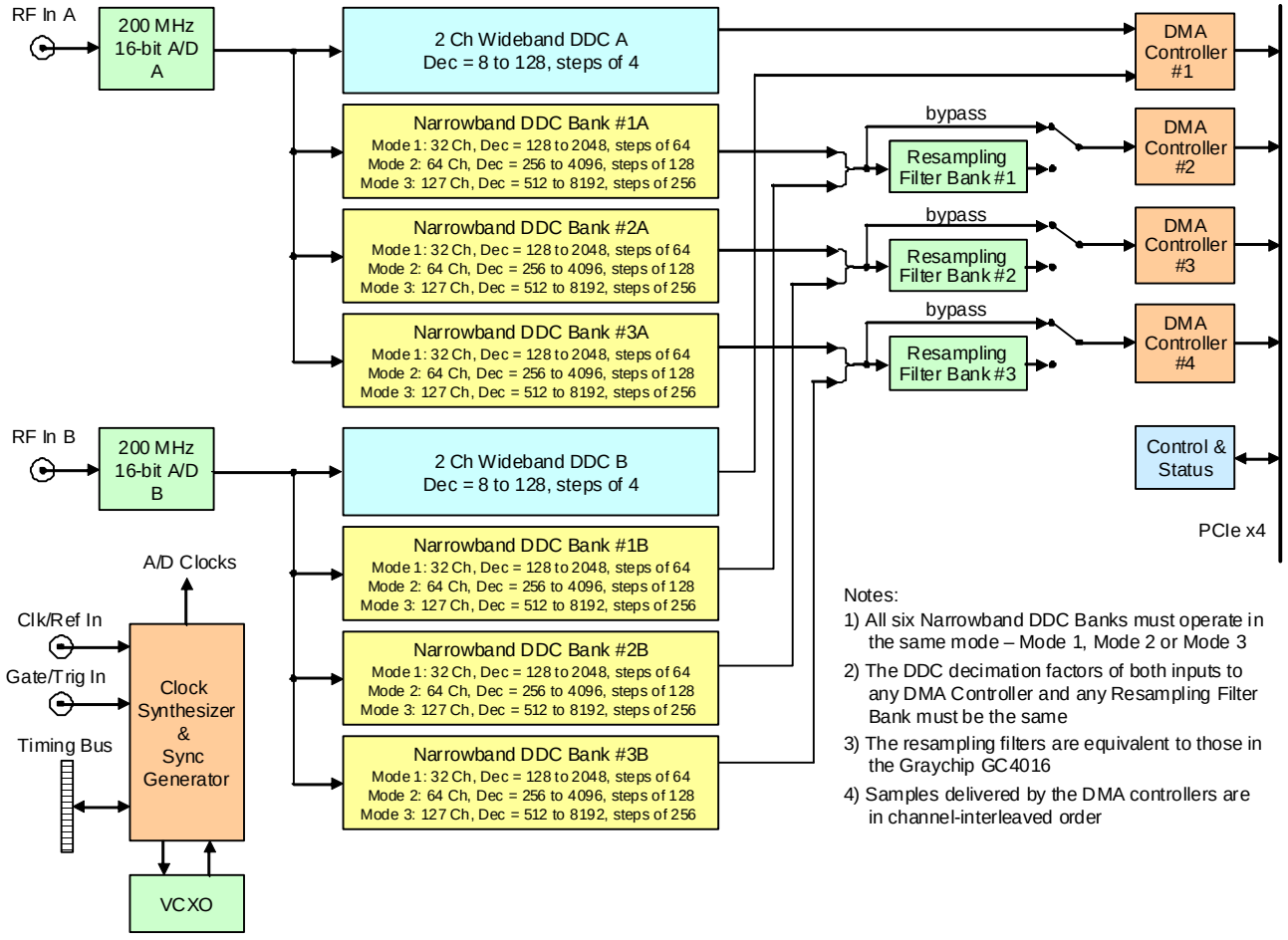
These modes are summarized in the following table:

Mode	Channels	Dec Range	Steps
1	32	128 - 2048	64
2	64	256 - 4096	128
3	127	512 - 8192	256

All six narrowband DDC banks must operate in the same mode.

The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers an output stream at a rate of f_s/N, and programmable for either 16-bit I + 16-bit Q, or 24-bit I + 24-bit Q complex samples. ➤



Notes:

1) All six Narrowband DDC Banks must operate in the same mode – Mode 1, Mode 2 or Mode 3
2) The DDC decimation factors of both inputs to any DMA Controller and any Resampling Filter Bank must be the same
3) The resampling filters are equivalent to those in the Graychip GC4016
4) Samples delivered by the DMA controllers are in channel-interleaved order

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Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

Narrowband DDCs (cont)

Because each pair of narrowband DDC banks feed a common DMA controller, the decimation setting for each DDC must be the same. Nevertheless, each pair can have a different decimation setting from the other pairs.

Resampling Filters

Three multiplexers allow outputs from each of the three narrowband DDC pairs to feed the associated DMA controller or feed the input of a resampling filter.

Each of the three resampling filters is an FIR lowpass filter that accepts DDC input samples at one sample rate and delivers output samples at another rate. Resampling filters are often used for better symbol recovery of signals using digital modulation schemes. The output rate is usually higher to create oversampling at a multiple of 2x, 4x, 8x, or 16x the symbol rate.

The resampling filter combines the operations of an FIR interpolation filter followed by a decimator. The overall resampling ratio is equal to the interpolation factor divided by the decimation factor, both of which are programmable parameters.

Note that each of the three resampling filters can be programmed independently. Some limitations on the DDC output data rates and subsequent resampling ratios may be imposed because of maximum PCIe transfer rates.

A/D Converters

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front-panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

The Model 52865 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Navigator BSP

Pentek's Navigator BSP provides a full suite of high-level C-callable libraries that support all features of the 52865 and demonstrate all of its functional modes with examples. The software package includes complete source code allowing the user to modify and integrate this functionality into the end application.

Navigator BSP also includes an extremely useful Signal Viewer utility that allows developers to view digitized signals from the output samples of any DDC in time and frequency domain.

Navigator BSP is available in versions for either Windows or Linux operating systems. ➤

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SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek board-level products. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed. The system is equipped with sufficient power and cooling to ensure optimum performance.

Ordering Information

Model	Description
52865	2-Channel 200 MHz A/D with 4 WB DDCs, 762 NB DDCs, Kintex UltraScale FPGA - 3U VPX
Options:	
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Wideband Digital Downconverters
- **Quantity:** Four
- **Decimation Range:** 8 to 128 in steps of 4, common to all four DDCs
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output
- **FIR Filter Performance:** 80% bandwidth <0.3 dB passband ripple, >100 dB stopband attenuation

Narrowband Digital Downconverters
- **Quantity:** Six banks
- **DDC Bank Modes:**
  - Mode 1: 32 DDCs, Dec = 128 to 2048, in steps of 64
  - Mode 2: 64 DDCs, Dec = 256 to 4096, steps of 128
  - Mode 3: 127 DDCs, Dec = 512 to 8192, steps of 256
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, with independent tuning for each channel
- **LO SFDR:** >120 dB
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4

Environmental
- **Standard: L0 (air cooled)**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
- **Option -702: L2 (air cooled)**
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
- **Option -713: L3 (conduction cooled)**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
- **Relative Humidity in all cases:** 0 to 95%, non-condensing

Size: 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

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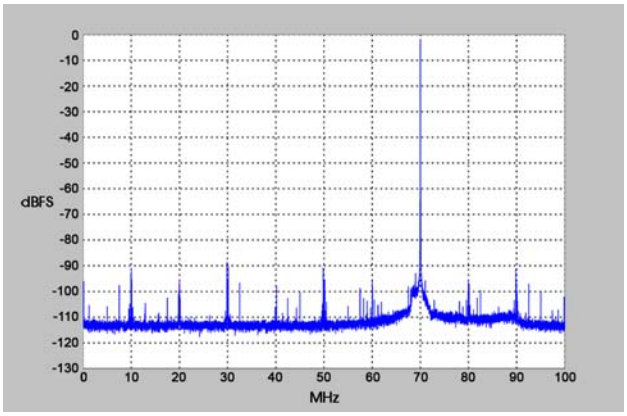
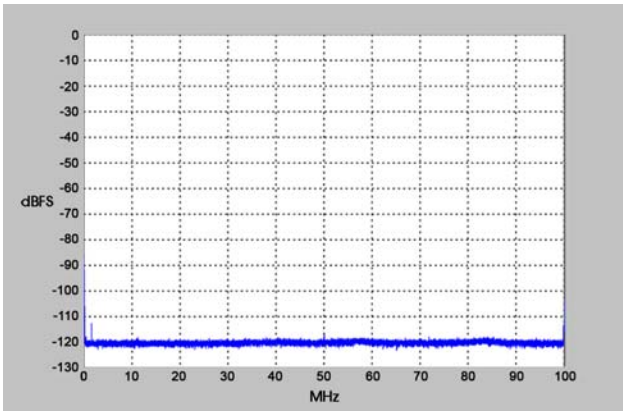
A/D Performance

Spurious Free Dynamic Range



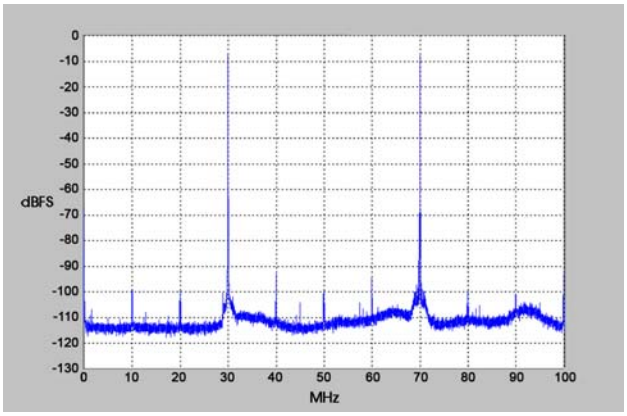
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



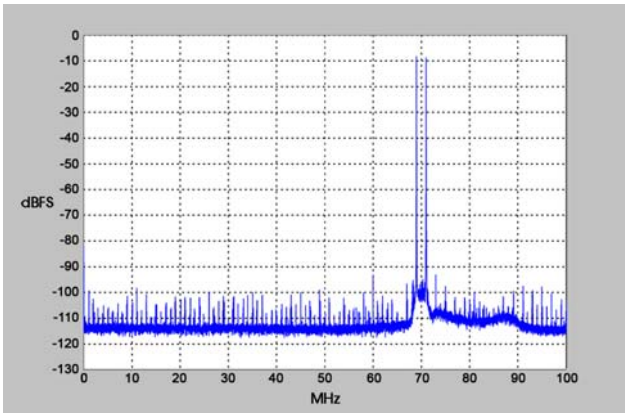
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



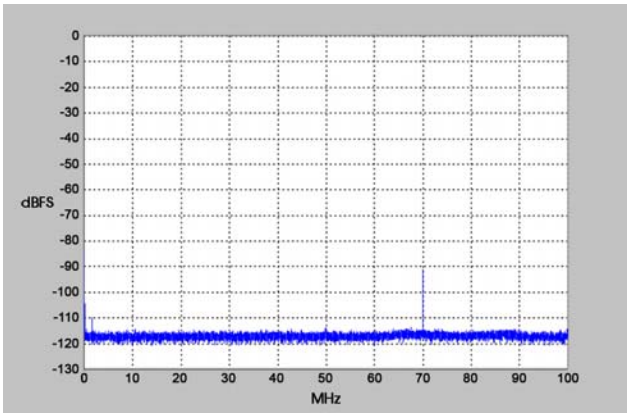
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



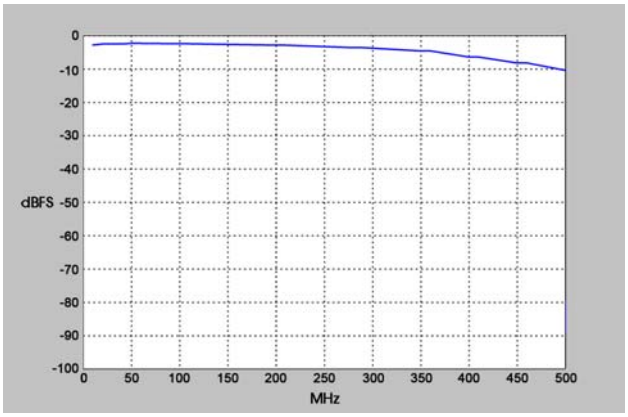
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk



$f_{in\ Ch2}$ = 70 MHz, f_s = 200 MHz, Ch 1 shown

Input Frequency Response



f_s = 200 MHz, Internal Clock