PENTEK

JADE KINTEX ULTRASCALE FPGA BROCHURE

The Latest Generations of Xilinx FPGAs

With each new generation of FPGA devices, Xilinx continues to push the performance envelope to match the ever increasing requirements of target applications.

The announcement of the Ultrascale was no exception. More processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements, are all part of these new devices.

While it might be easy to assume that faster, bigger, more powerful is better, it's important to understand how the latest FPGA innovations actually deliver this higher performance to best match the device to the specific requirements of the application.

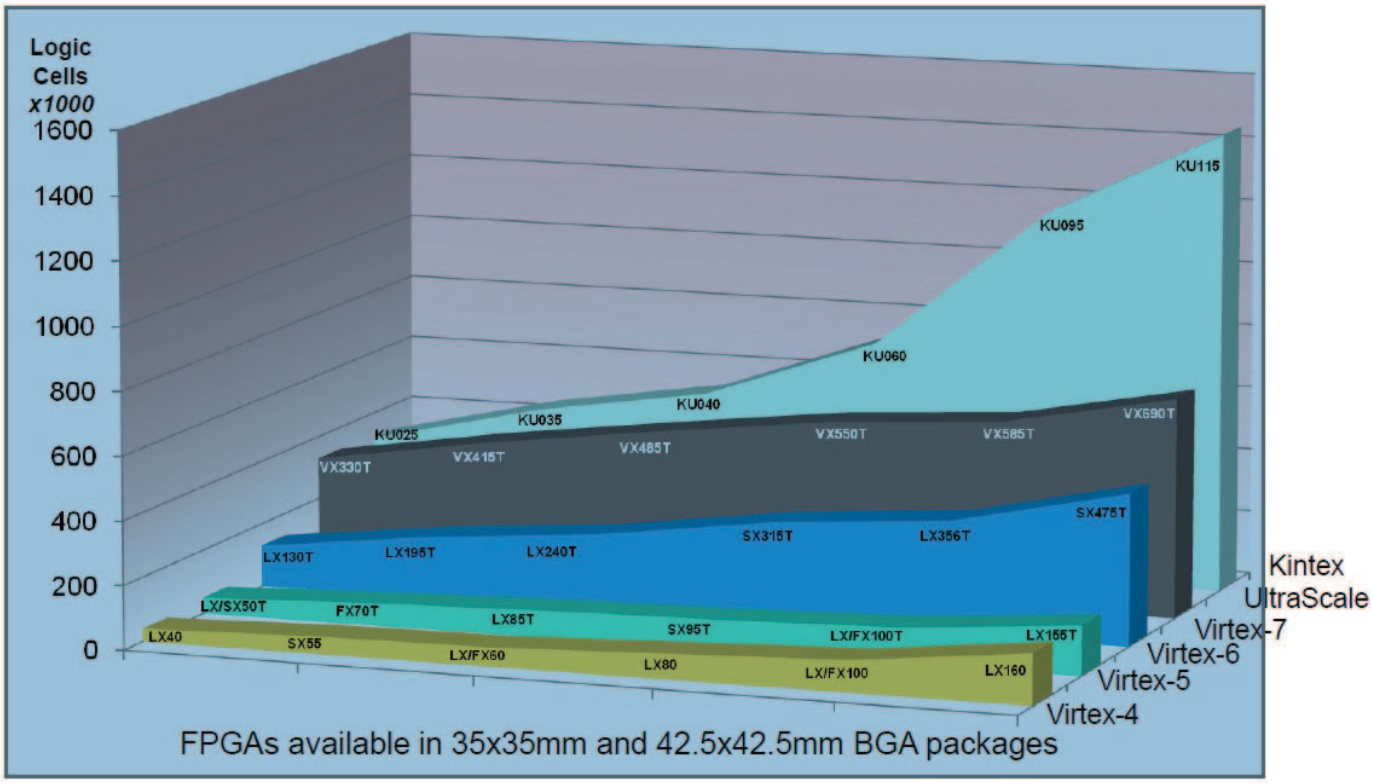
One of the standard metrics for FPGAs is the number of logic cells. This figure shows the steady improvement in the last five generations of Xilinx FPGAs starting with the Virtex-4 and continuing to the Kintex Ultrascale. The graph displays the number of logic cells contained in a range of different density devices offered in a 35 mm x 35 mm BGA (Ball-Grid Array) package. This clearly shows the dramatic increase in resource density, bounded by the constraints of the size and power dissipation capacity of a given package.

Kintex® UltraScale™ devices provide the best price/performance/watt balance, delivering the most cost-effective solution for high-end capabilities including transceiver and memory interface line rates. The newest mid-range family is ideal for both packet processing and DSP-intensive functions, and is well suited for applications ranging from wireless MIMO technology to high-bandwidth networking and data center. This combination of lower power and higher performance for each of the key resources benefits software radio, opens up new product markets, and extends the capabilities of existing applications.

XILINX
ALLIANCE PROGRAM
CERTIFIED

As a Certified Member of Xilinx's Alliance program, Pentek has passed a comprehensive 320-point review of its technical, business, quality, and support processes and has committed engineers who completed the same rigorous training used by Xilinx Field Application Engineers worldwide.

Pentek continues to demonstrate years of expertise with Xilinx devices and implementation techniques that consistently deliver high-quality products and services utilizing the Xilinx programmable platforms.



Logic Cell Density Comparison, Virtex-4, Virtex-5, Virtex-6, Virtex-7 and Kintex Ultrascale FPGAs Used in Pentek Products

Board-Level Products for High-Performance Applications

Inside the Heart of Jade

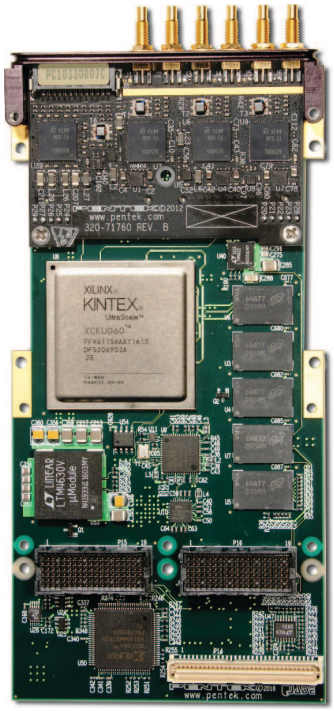
The Pentek Jade architecture is based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by over 50% with equally impressive reductions in power dissipation, and cost.

As the central feature of the Jade Architecture, the FPGA has access to all data and control paths, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control. The Gen 3 x8 PCIe link can sustain with peak transfers of 8 GB/sec data transfers to system memory. Eight additional serial gigabit lanes and LVDS general purpose I/O lines are available for custom applications.

The Jade architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

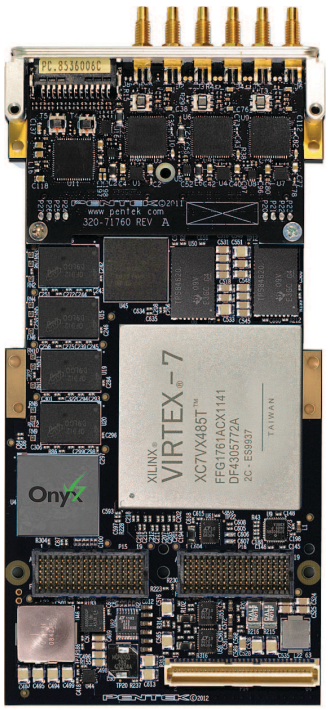
Performance Features

- Jade™: Xilinx Kintex Ultrascale FPGA
- A/D sampling rates from 10 MHz to 6.4 GHz
- D/A sampling rates up to 6.4 GHz
- Powerful linked-list DMA engines
- PCI Express as the primary control and data-transfer interface
- On-board clocking and synchronization
- I/O to support a wide range of signal types
- Secondary serial gigabit interface
- Available in commercial and in several ruggedization levels up to and including conduction cooling



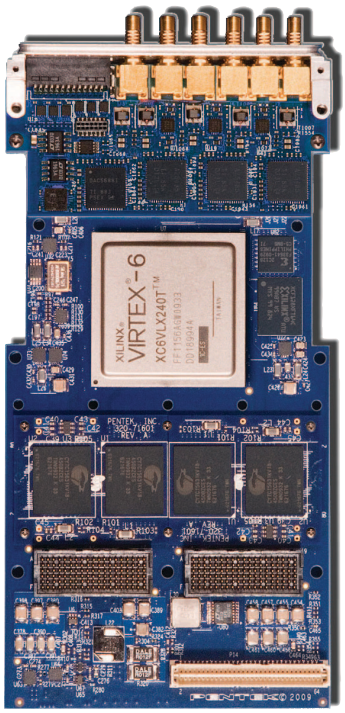
Jade

Kintex UltraScale, XMC Configuration



Onyx

Virtex-7, XMC Configuration



Cobalt

Virtex-6, XMC Configuration

With over 300 boards to choose from, engineers can find both commercial and rugged versions of the I/O boards best suited for their application.

Each family of FPGA boards boost memory, logic and I/O performance. All Jade, Onyx and Cobalt boards are available in XMC, 3U and 6U VPX, AMC and 3U and 6U cPCI form factors.

Components and Circuitry

The Jade Module

Shown here is a typical Jade module. The input analog ports are transformer-coupled to two high-speed A/D converters. Their digital outputs are delivered into the Kintex Ultrascale FPGA for signal processing, data capture or for routing to other module resources.

Besides the two A/Ds, the typical module could include one DUC (Digital Upconverter) and two D/As which are transformer-coupled to the output analog ports.

In addition to the input and output ports, the module includes a multipin connector for clocking and synchronization. All connectors are conveniently located on the front panel.

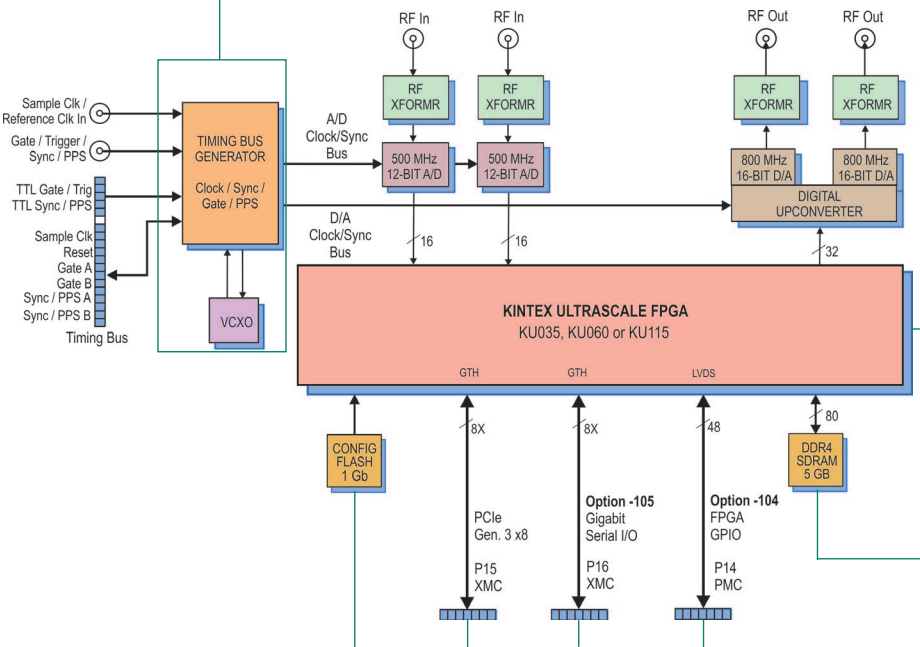
Clocking and Synchronization

The internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

The timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock which can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the synthesizer locks the VCXO to an external system reference, typically 10 MHz.

A front panel Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts inputs that drive the clock, sync and gate signals. In the master mode, it can drive the timing signals for synchronizing multiple boards.



Xilinx FPGAs

The Jade Kintex Ultrascale FPGA can be populated with one of three different FPGAs to match the specific requirements of the processing task. Supported FPGAs are the KU035, KU060, or the KU115.

The KU115 device is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

If the application is less demanding, one of the other two lower cost devices may be installed.

Storage Resources

Memory for the Jade product line consists of a large 5 GByte bank of DDR4 SDRAM.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

FLASH Memory

The 16-bit-wide 1 Gb FLASH provides non-volatile memory for factory boot code, self-test, and user parameters.

Board Interfaces

The FPGA is also used to implement the primary board interfaces. The basic XMC module shown here is also available in different form factors, such as PCI Express, VPX, and CompactPCI.

More information about form factors and interfaces starts on the page 7.

The Jade Architecture

FPGA Dataflow

All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering, and memory control. The Jade Architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. Depending on model, the factory-installed functions may include A/D acquisition and D/A waveform generator IP modules. IP modules for memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the board to operate as a complete turnkey solution without the need to develop any FPGA IP.

For applications that require specialized functions, users can install custom IP for data processing. Pentek Navigator® FPGA Design Kits (described later in this brochure) include all of the factory- installed modules delivered as IP blocks.

A/D Acquisition IP Modules

This typical Jade IP design includes two A/D Acquisition IP modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

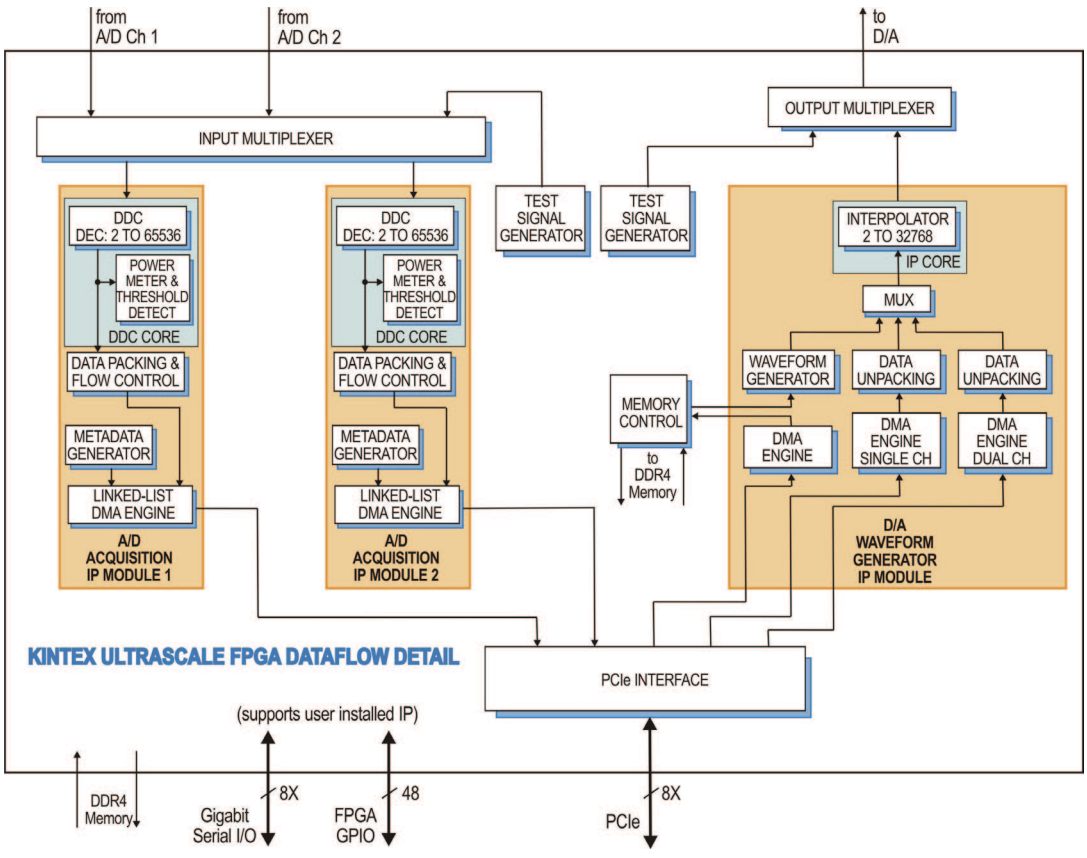
For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Generator IP Module

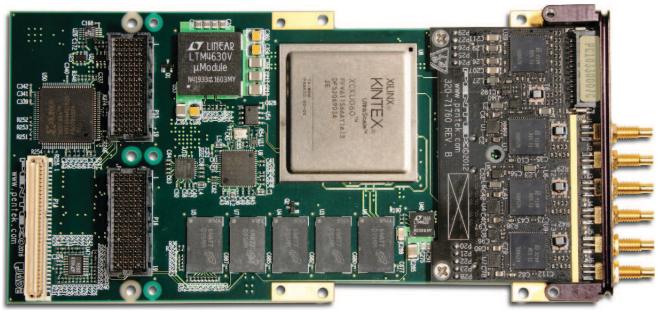
Factory-installed functions for this typical Jade board include a D/A waveform generator IP module. A linked-list controller allows users to easily output waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

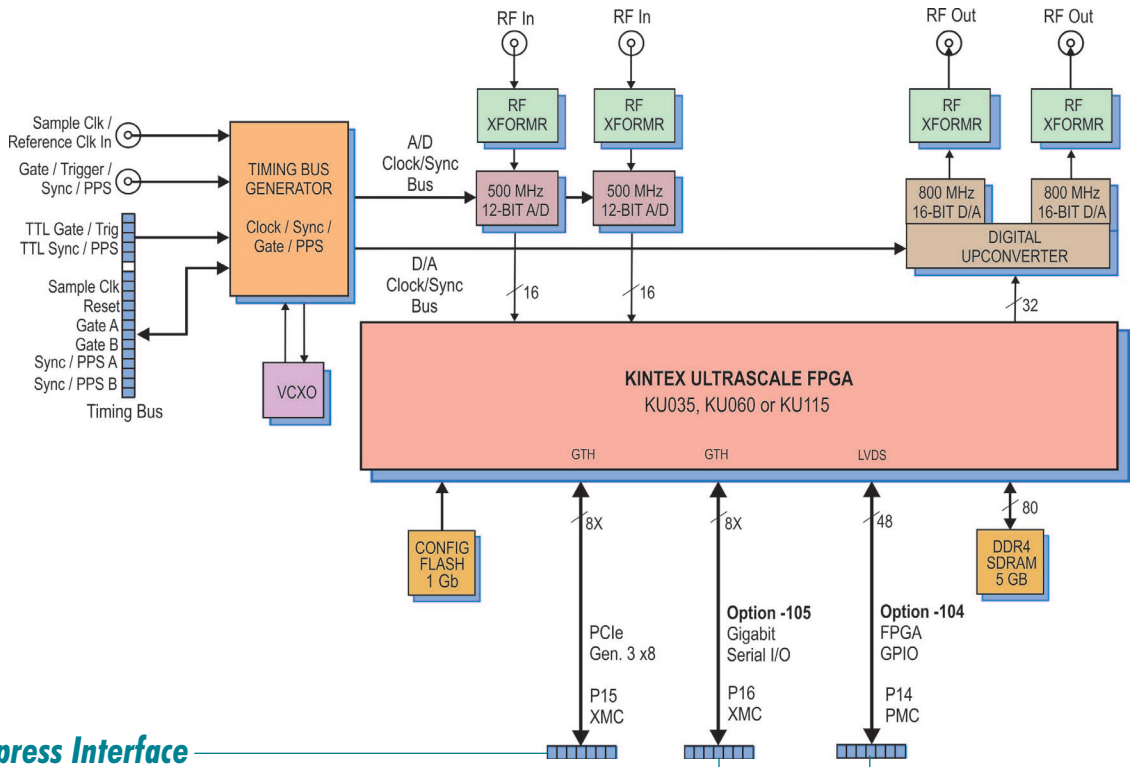


XMC - 71xxx Series



XMC Module

In its XMC configuration, each module complies with the VITA 42.0 XMC specification and is suitable for mounting on processor boards with XMC connectors. All XMC modules are available in commercial and in several ruggedization levels up to and including conduction cooling.



PCI Express Interface

The XMC form factor includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications. Gen 3 provides 8 GB/sec peak data transfer rate

The PCIe interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

Jade XMC products comply with the VITA 42.0 XMC specification. Each of two connectors provides a 8X link.

With dual XMC connectors, the XMC products support both x4 and x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Optional Interfaces

Option -104 installs the P14 PMC connector with 24 signal pairs to the FPGA for custom I/O.

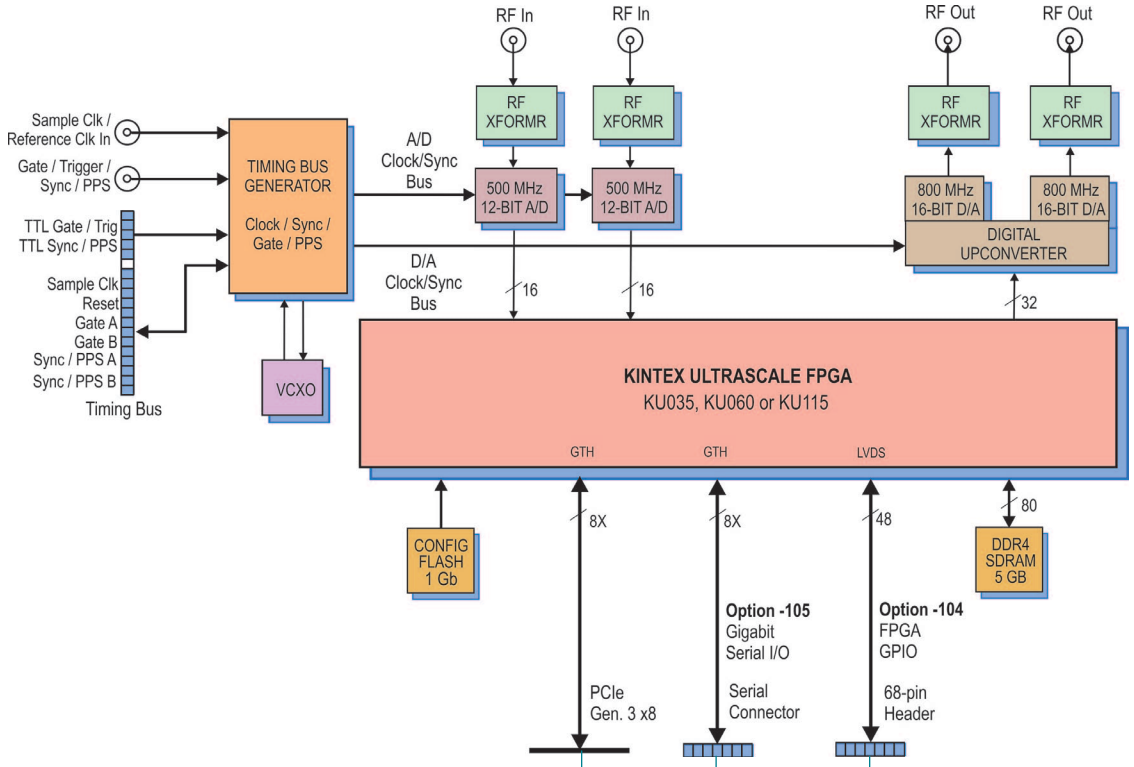
Option -105 installs the P16 XMC connector with a 8X gigabit link to the FPGA to support serial protocols for all products.

Jade Form Factors & Interfaces

PCIe - 78xxx Series

x8 PCIe Board

The PCI Express form factor is suitable for mounting in PCs with PCIe connectors and interfaces. Physically, the XMC module reviewed in the previous page is mounted on a PCI Express "carrier" board with x8 PCIe motherboard connectors. Other connectors on this board provide additional interfaces as described below. The unique design of the PCIe carrier includes an integrated fan that keeps the module cool even in demanding situations while requiring a single PCIe slot.



PCI Express Interface

The PCIe board includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications. Gen. 3 provides 8 GB/sec peak transfer rate.

The PCIe interface includes multiple DMA controllers for efficient transfers to and from the module.

Optional Interfaces

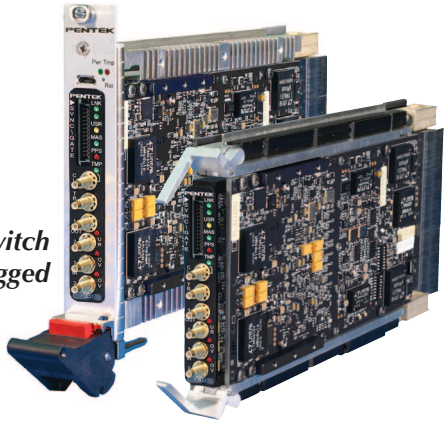
Option -104 connects 24 pairs of LVDS connections from the FPGA to a 68-pin ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects an 8X gigabit serial links from the FPGA to an 8X gigabit serial connector along the top edge of the PCIe board for custom I/O.

SPARK Development Systems

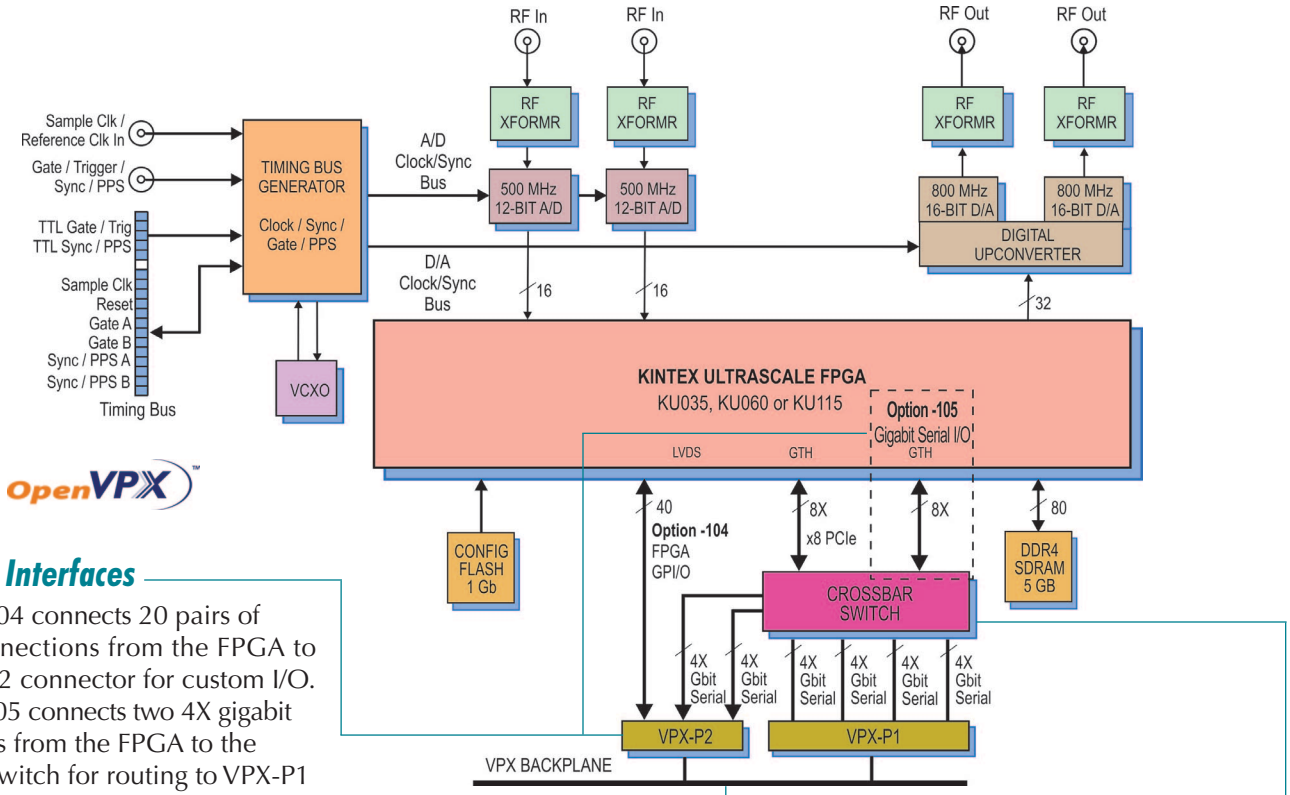
The SPARK® product family are integrated development systems for Pentek software-defined radio (SDR) and data acquisition boards. The SPARK series was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

3U VPX - 53xxx Series



3U VPX Boards with crossbar switch
Commercial (left) & Rugged

The 3U VPX form factor is compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65*. The 53xxx Series mounts one XMC module on a 3U VPX carrier with a flexible crossbar switch. It is available in commercial air-cooled and ruggedized versions up to and including conduction cooling. See Table 1 for a comparison with the 52xxx Series described on the next page.



Optional Interfaces

Option -104 connects 20 pairs of LVDS connections from the FPGA to the VPX P2 connector for custom I/O. Option -105 connects two 4X gigabit serial links from the FPGA to the crossbar switch for routing to VPX-P1 and VPX-P2.

Table 1: 3U VPX Family Comparison

	52xxx Series	53xxx Series
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option-104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option-105 path	x8 on VPX P1	x8 on VPX P1 and/or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

PCI Express Interface

The 3U VPX board includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Gen. 2 x8 provides 4 GB/sec peak transfer rate.

The PCIe interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 3U VPX Jade board features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X) for routing over to the VPX-P1 and/or VPX-P2 connector.

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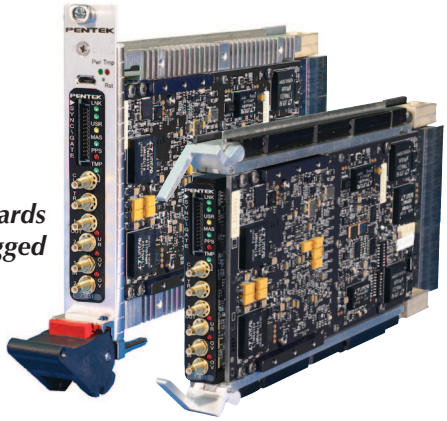
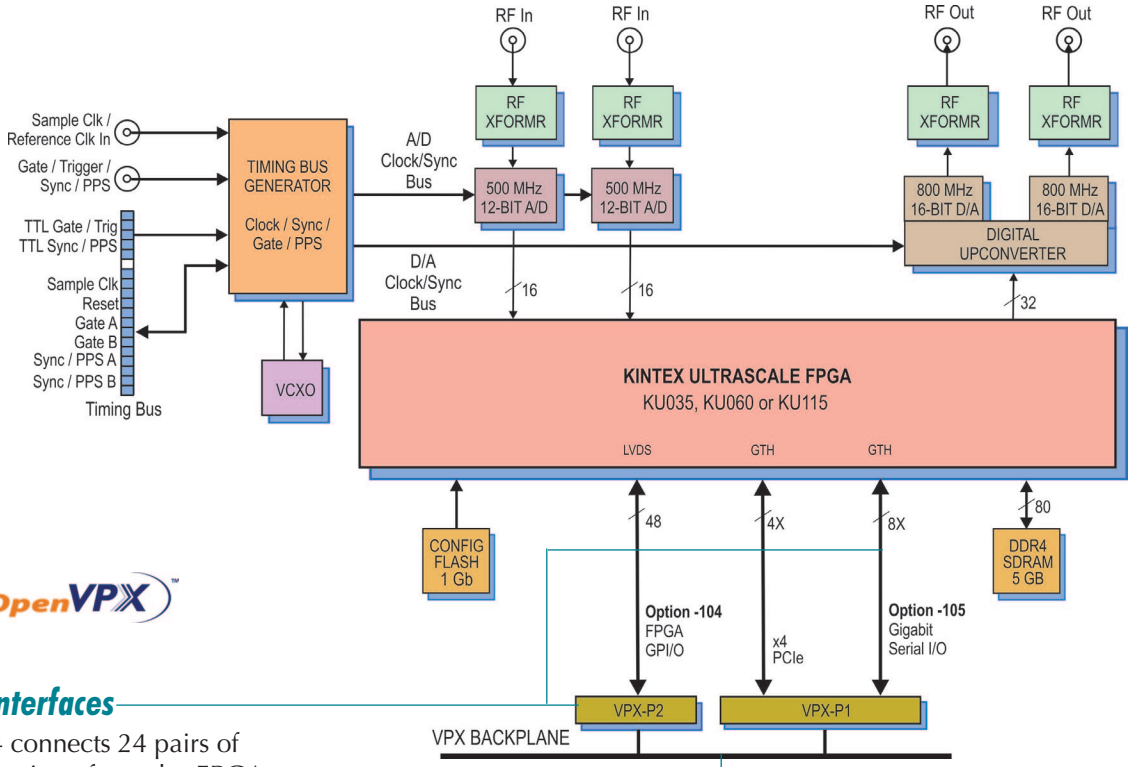
Jade Form Factors & Interfaces

3U VPX - 52xxx Series



3U VPX Boards
Commercial (left) & Rugged

The 3U VPX form factor is also compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 OpenVPX™*. The 52xxx Series mounts one XMC module on a simple, low cost 3U VPX carrier with no crossbar switch. It is available in commercial air-cooled and ruggedized versions up to and including conduction cooling. See Table 1 on the previous page for a comparison with the 53xxx Series.



OpenVPX™

Optional Interfaces

Option -104 connects 24 pairs of LVDS connections from the FPGA to the VPX P2 connector for custom I/O.

Option -105 connects an 8X gigabit serial link from the FPGA to VPX-P1.

PCI Express Interface

The 3U VPX board includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications. Gen. 3 provides 4 GB/sec peak transfer rate.

The PCIe interface includes multiple DMA controllers for efficient transfers to and from the board.

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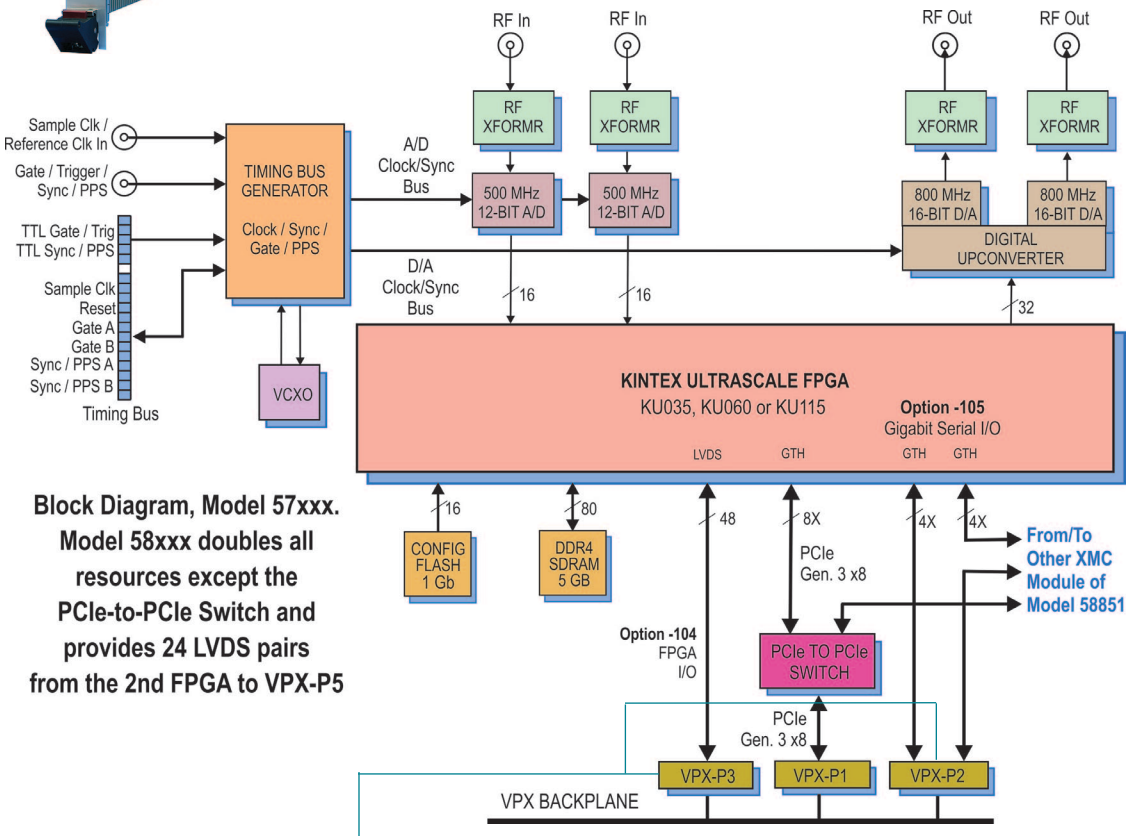
6U VPX - 57xxx & 58xxx Series

6U VPX
58xxx Series board

The 6U VPX form factor is also compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 OpenVPX™*. The 58xxx Series mounts two XMC modules on a 6U VPX carrier, while the 57xxx Series mounts only one. Both series are available in commercial air-cooled and ruggedized versions up to and including conduction cooling.



Block Diagram, Model 57xxx. Model 58xxx doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

Optional Interfaces

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57851; and 24 pairs each to P3 and P5 connectors, Model 58851.

Option -105 installs additional gigabit serial lanes. On the 57xxx, a single 4x interface is provided to the VPX-P2, on the 58851 a 4x interface is provided from each FPGA to the VPX-P2 and an addition 4x interface is provided between the two FPGAs. Users can install their own serial protocol IP to utilize these interfaces.

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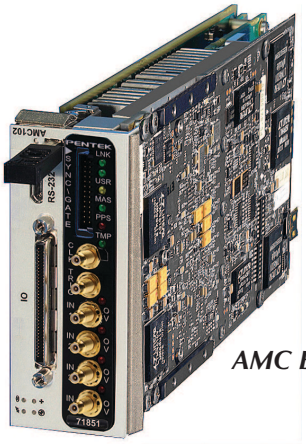
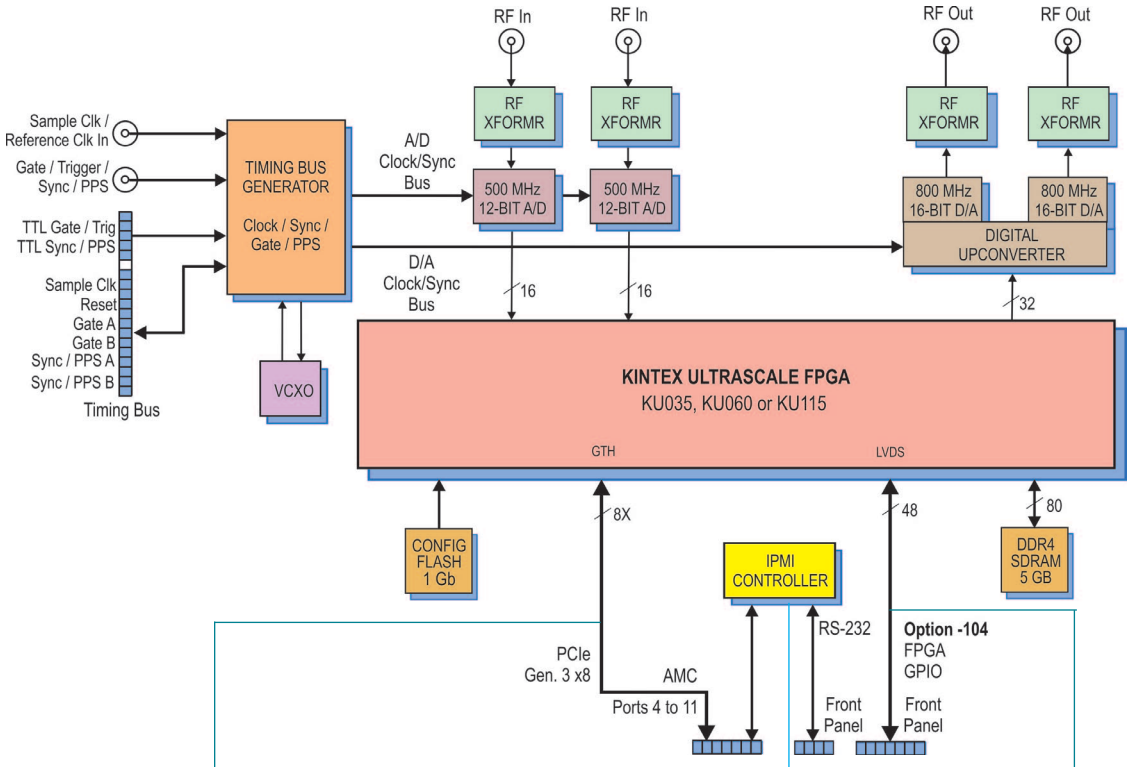
AMC - 56xxx Series



AMC Board

The AMC 56xxx Series complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).



PCI Express Interface

The AMC module includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 & 3 bus specifications.

The x8 PCIe interface includes multiple DMA controllers for efficient transfers to and from the board.

Module Management

The Module Management Controller complies with the IPMI 2.0 MMC specification.

Optional Interface

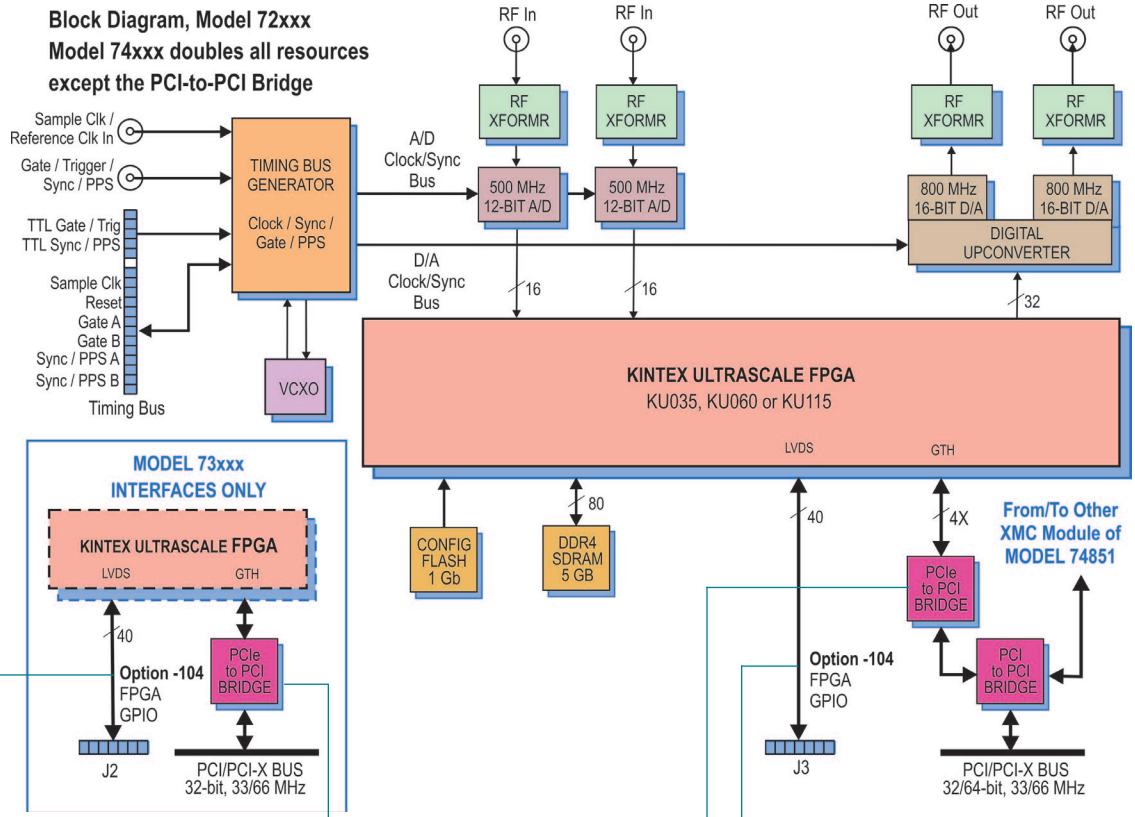
Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Compact PCI - 72xxx, 73xxx & 74xxx Series

6U cPCI 74xxx Series board

3U cPCI 73xxx Series board

The CompactPCI form factor is available in three configurations. The 6U cPCI 72xxx Series mounts two XMC modules on a 6U carrier board. The 6U cPCI 74xxx Series mounts only one XMC module on a 6U carrier board. The 3U cPCI 73xxx Series mounts one XMC module on a 3U carrier board.



3U cPCI 73xxx Single XMC

A PCIe-to-PCI bridge connects the x4 PCIe interface from the XMC module to the 32-bit, 33/66 MHz PCI/PCI-X bus.

6U cPCI 74xxx Dual XMC

Two PCIe-to-PCI bridges connect the x4 PCIe interfaces from each XMC module to a PCI-to-PCI bridge. This bridge connects both modules to the 32- or 64-bit, 33/66 MHz PCI/PCI-X bus.

6U cPCI Optional Interface

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J3 connector for custom I/O. The J5 connector supports Option -104 for the 2nd XMC module.

3U cPCI Optional Interface

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J2 connector for custom I/O.

6U cPCI 72xxx Single XMC

The 2nd XMC module, its associated PCIe-to-PCI bridge and the optional interface connection to J5 are not present.

Software Support

NAVIGATOR
Design Suite

JADE

VIVADO

Navigator Design Suite Streamlines Development

Pentek's Navigator Design Suite includes the Navigator FDK (FPGA Design Kit) for integrating custom IP into the Pentek factory-shipped design and the Navigator BSP (Board Support Package) for creating host applications. The Navigator Design Suite takes a new approach to solving FPGA IP and control software connectivity.

Most modern FPGA-processing applications require development of specialized FPGA IP to run on the hardware, ***and*** software to control the FPGA hardware from a host computer.

Even when "turnkey" solutions are delivered with complete FPGA IP and software libraries, as developers add their own custom-processing IP, new software needs to be created to control the custom IP functions.

Problems often arise when the IP and software development tools treat application development as two separate tasks. Changes to FPGA IP and control software can quickly get out of sync, complicating new application development or even breaking the formally functioning turnkey components.

The Navigator Design Suite was designed from the ground up to work with Pentek's Jade™ architecture and provide a better solution to the complex task of IP and software creation.

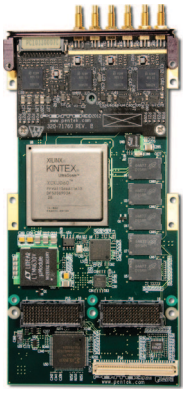
Navigator FDK (FPGA Design Kit) for Custom FPGA Design

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater.

The Xilinx Vivado Design Suite includes IP Integrator, the industry's first plug-and-play IP integration design environment. Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek's Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

Each Navigator FDK provides the complete IP for a specific Jade data acquisition and processing board. When the design is opened in Vivado's IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application. All blocks use industry standard AXI4 interfaces providing a well-defined format for custom IP to connect to the rest of the design. Each Navigator/Jade design includes User Blocks in the data-flow path, ideal for inserting custom processing IP.

The Navigator FDK includes complete documentation, test benches and full VHDL source for developers who desire complete access to the IP. In addition to the IP specific to the supported Jade board, Navigator also includes processing blocks for some of the most commonly used algorithms.

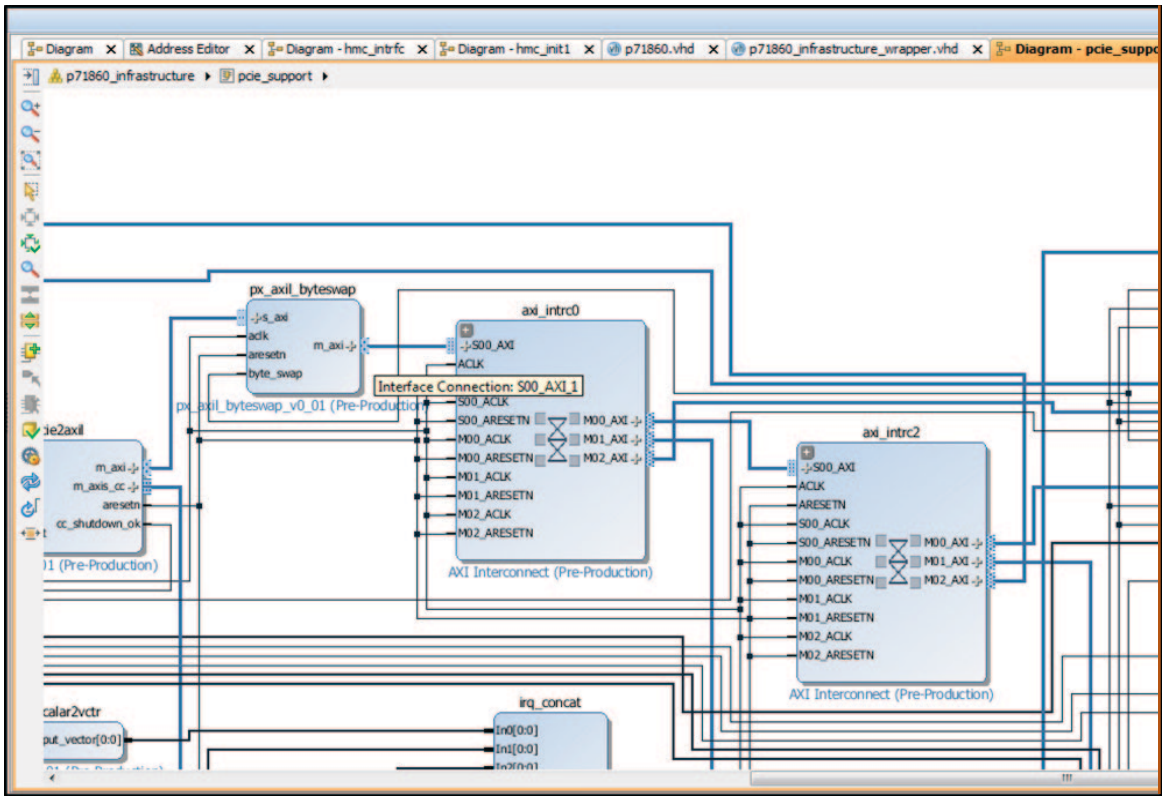


Model 71851

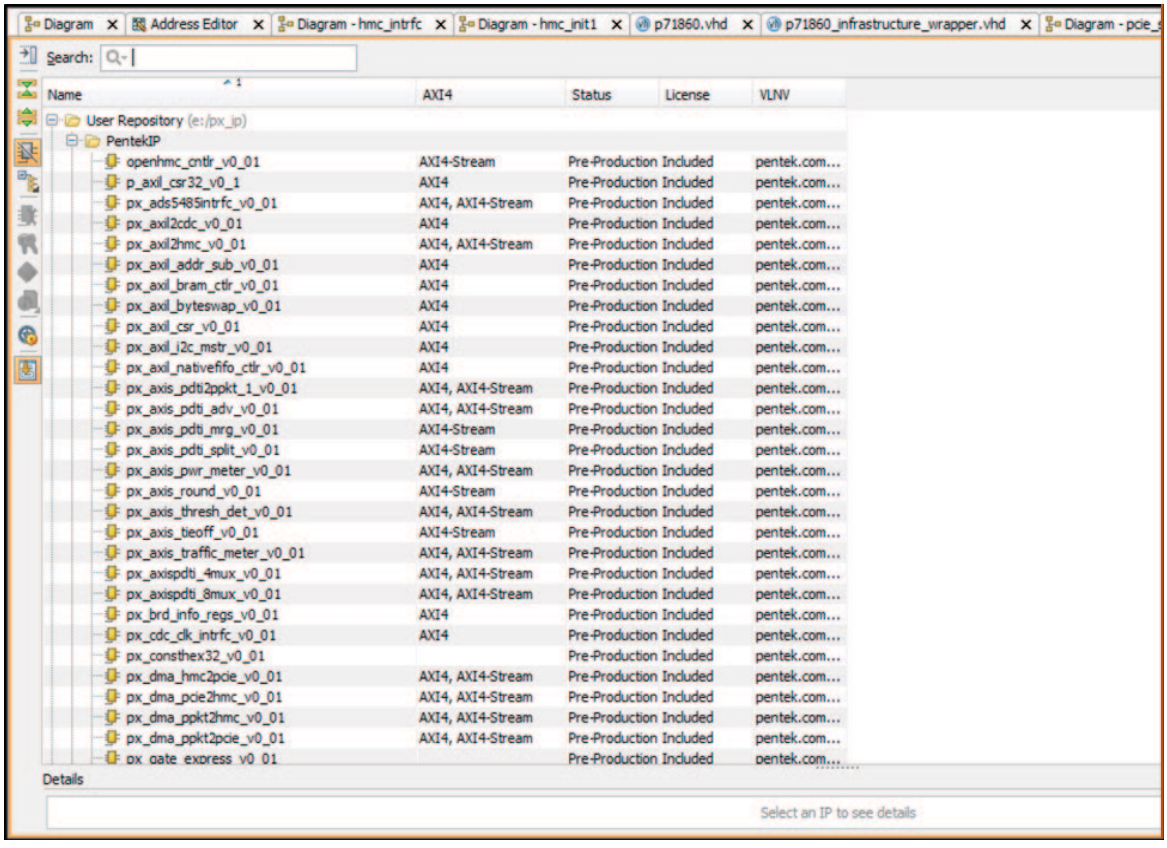
2-Chan 500 MHz A/D with DDC & 2-Chan 800 MHz D/A with DUC, Kintex UltraScale - XMC

Available in the form factors described in the previous pages, the Model 71851 is a member of the Jade family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today. Designed to work with the Pentek new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

NAVIGATOR
Design Suite



Built around a graphical block diagram interface, IP Integrator allows developers to leverage existing IP by importing it into their block diagram design.



All Pentek Navigator FDK IP blocks can be selected from pull-down menus within IP Integrator.

Software Support

NAVIGATOR
Design Suite

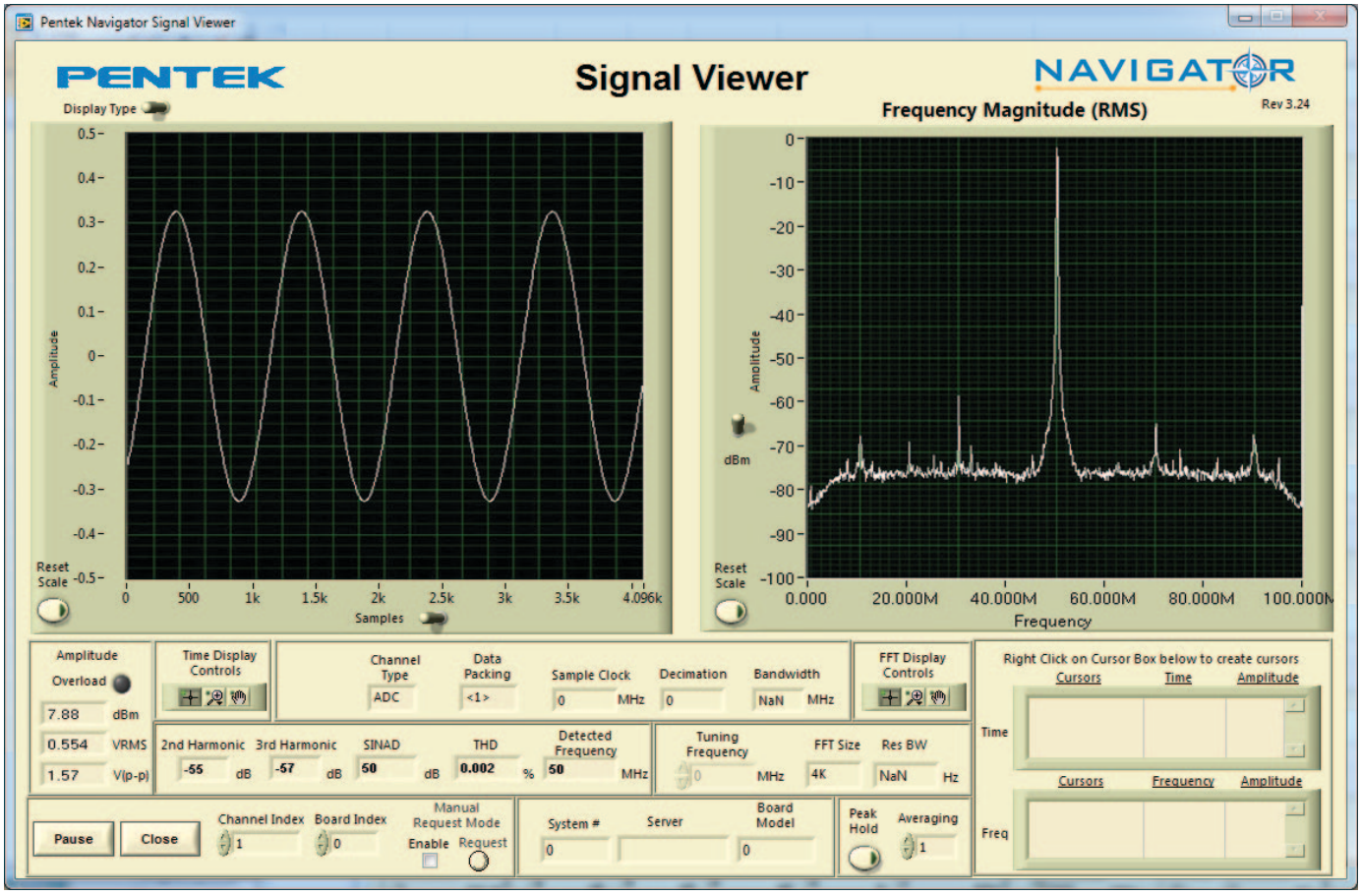
Navigator BSP (Board Support Package) Enables Hardware Control

The companion product to the Navigator FDK is the Pentek Navigator Board Support Package (BSP). While Navigator FDK provides a streamlined path for modifying or creating new IP for the Pentek hardware, the Navigator BSP enables complete operational control of the hardware and all IP functions in the FPGA.

Similar to the FDK, the BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an intuitive API. The API allows developers to focus on the task of creating the application by letting the API, the hardware and IP-control libraries below it to handle many of the board-specific functions. Developers who want full access to the entire BSP library, enjoy complete C-language source code as well as full documentation.

New applications can be developed on their own or by building on one of the included example programs. All Jade boards are shipped with a full suite of build-in functions allowing operation without the need for any custom IP development. Many users find these functions ideal for addressing their application requirements.

The Navigator BSP includes the Signal Analyzer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Analyzer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.



Navigator BSP Signal Analyzer

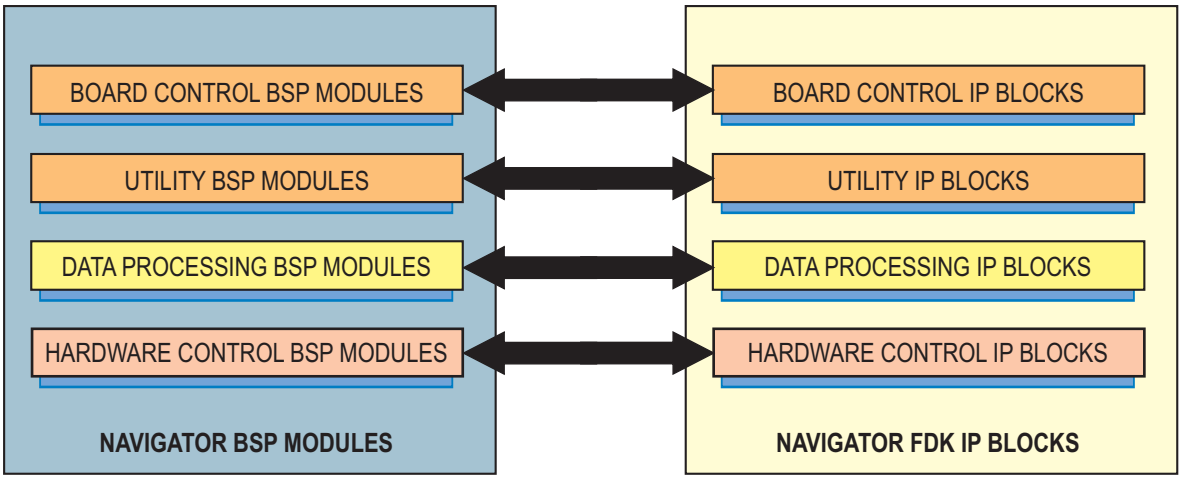
NAVIGATOR
Design Suite

Optimize BSP and IP Development

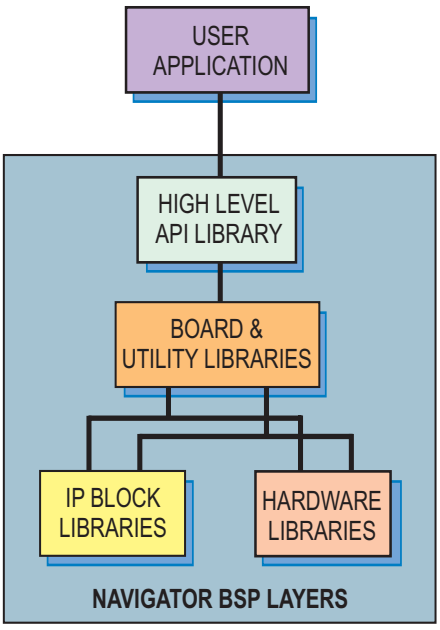
For users who need to develop applications that include custom IP, the combination and compatibility of Navigator FDK and Navigator BSP streamline development.

When new IP is introduced into the design, it has the potential of changing how the hardware looks to the host, possibly breaking the software. Navigator FDK and BSP were designed together to closely match the FPGA IP blocks and the BSP functions that control them. As developers modify IP they can easily find the corresponding BSP functions and modify them in parallel.

Navigator FDK uses AXI4 for all IP block interfaces. When developers create their own IP blocks using AXI4, they are immediately compatible with the Pentek-supplied IP. Following the Navigator BSP style guide, users can similarly create BSP modules for compatibility with the Navigator BSP library.



For users who need to develop applications that include custom IP, the combination and compatibility of Navigator FDK and Navigator BSP streamline development.



The Navigator BSP allows software developers to operate at the level most appropriate for their application requirements, from the high level API to control most functions to the hardware and IP block libraries for access to individual registers.

"Our new Jade architecture gives our customers unprecedented levels of performance at significantly lower product cost," said Rodger Hosking, vice president of Pentek. "We also developed new software development tools to align with the latest industry standards and Xilinx development tools, providing a more intuitive and productive development environment."

Jade XMC Selection Chart

JADE	A/D Converters Qty	A/D Converters Rate	A/D Converters Bits	D/A Converters Qty	D/A Converters Rate	D/A Converters Bits	Other Features
71141	1/2	6.4/3.2 GHz	12	2	6.4 GHz	14	DDCs & DUCs
71841	1/2	3.6/1.8 GHz	12				DDCs
71851	2	500 MHz	12	2	800 MHz	16	DDCs & Inter.
71132	8	250 MHz	16				8WB, 64 MB DDCs
71131	8	250 MHz	16				8 DDCs
71862	4	200 MHz	16				4 WB, 32 MB DDCs
71861	4	200 MHz	16				4 DDCs
71821	3	200 MHz	16	2	800 GHz	16	3 DDCs & 2 DUCs

Rate = Max Sampling Frequency
Inter. = Interpolation Filter

DDC = Digital Downconverter
DUC = Digital Upconverter
WB = Wideband
MB = Multiband

Model Number	Form Factor	Number of XMCs
71xxx	XMC	1
72xxx	6U cPCI	1
73xxx	3U cPCI	1
74xxx	6U cPCI	2
78xxx	PCIe Half Length	1
52xxx	3U VPX	1
53xxx	3U VPX	1
57xxx	6U VPX	1
58xxx	6U VPX	2
56xxx	AMC	1

First 2 digits determine form factor

Jade Software Support

NAVIGATOR Design Suite	Description
4811	Navigator FDK: FPGA Design Kit
4814	Navigator BSP: Board Support Package for Linux
4815	Navigator BSP: Board Support Package for Windows

PENTEK

Setting the Standard for Digital Signal Processing

JADE

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