PENTEK

JADE

The Jade Family

The Jade® family of board-level products is based on the Xilinx Kintex UltraScale FPGAs. Jade includes products for radar, software radio, and communications based on these FPGAs.

Form Factors

All products in the Jade family are available in the following form factors:

- XMC
- x8 PCI Express
- AMC
- 3U OpenVPX
- 6U OpenVPX
- 3U CompactPCI
- 6U CompactPCI

The Jade Architecture

The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's Navigator® Design Suite, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. Typical factory-installed functions may include A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the board to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Synchronization

An internal timing bus provides board timing and synchronization. The bus includes a clock, sync and gate or trigger signals. A Clock/Sync connector allows multiple boards to be synchronized. Multiple boards can be driven from the bus master, thereby supporting synchronous sampling and sync functions across all connected boards.

Ruggedization

Except for the PCIe form factor, all other boards are available in various ruggedized formats up to and including conduction cooling.

SPARK
Development Systems

The Pentek SPARK® systems are fully-integrated development systems for Pentek Cobalt, Onyx, Flexor, and Jade software radio, data acquisition and I/O boards. They save engineers and system integrators the time and expense of designing and building systems that ensure optimum performance of Pentek boards.

Each SPARK system is delivered with the Pentek board(s) and required software installed and is equipped with sufficient cooling and power to ensure optimum performance.
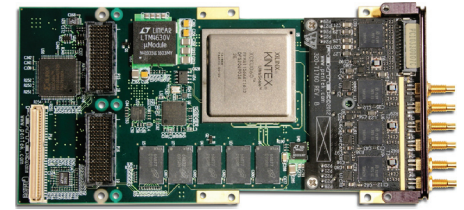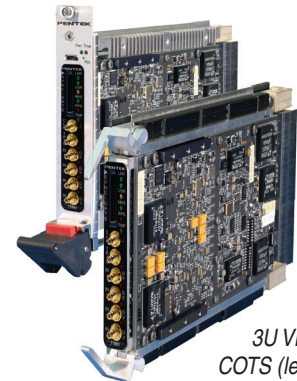

XMC Module
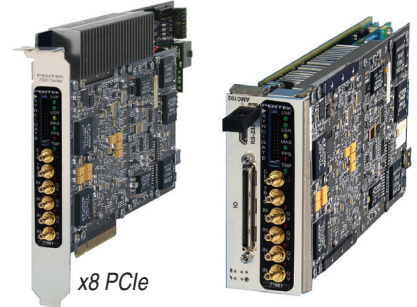
x8 PCIe

AMC

3U VPX COTS (left) and Rugged

3U cPCI

6U cPCI Double Density

6U VPX Double Density

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Pentek's Navigator® Design Suite includes the Navigator FDK (FPGA Design Kit) for integrating custom IP into the Pentek factory-shipped design and the Navigator BSP (Board Support Package) for creating host applications. Most modern FPGA-processing applications require development of specialized FPGA IP to run on the hardware, *and* software to control the FPGA hardware from a host computer.

The Navigator Design Suite was designed from the ground up to work with Pentek's Jade and Quartz architectures and provides a better solution to the complex task of IP and software creation.

Navigator FDK (FPGA Design Kit)

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater.

The Xilinx Vivado Design Suite includes IP Integrator, the industry's first plug-and-play IP integration design environment. Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek's Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

Each Navigator FDK provides the complete IP for a specific Jade or Quartz data acquisition and processing board. When the design is opened in Vivado's IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application.

Navigator BSP (Board Support Package)

The companion product to the Navigator FDK is the Pentek Navigator Board Support Package (BSP). While Navigator FDK provides a streamlined path for creating or modifying new IP for the Pentek hardware, the Navigator BSP enables complete operational control of the hardware and all IP functions in the FPGA.

Similar to the FDK, the BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an intuitive API. The API allows developers to focus on the task of creating the application by letting the API, the hardware and IP-control libraries below it to handle many of the board-specific functions. Developers who want full access to the entire BSP library, enjoy complete C-language source code as well as full documentation.

New applications can be developed on their own or by building on one of the included example programs. All Jade and Quartz boards are shipped with a full suite of build-in functions allowing operation without the need for any custom IP development.
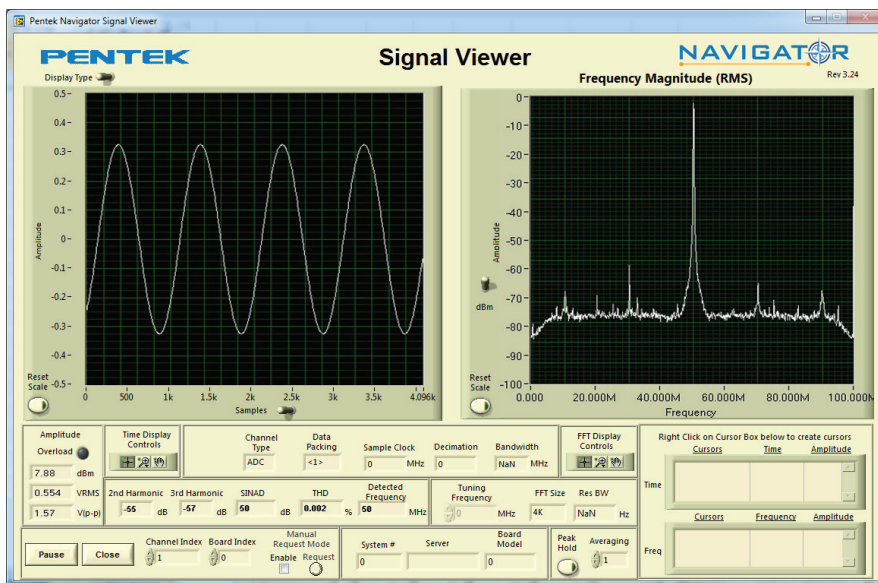
The Navigator BSP includes the Signal Analyzer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Analyzer, users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.